DDR2 VLP Registered MiniDIMM

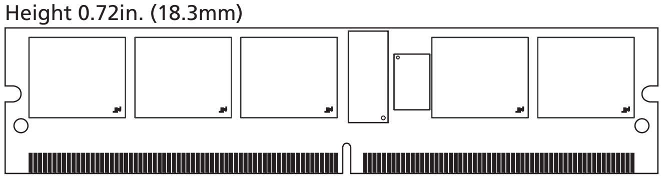
MT18HVS12872(P)K – 1GB

For component specifications, refer to Micron's Web site: www.micron.com/products/ddr2sdram

Features

- 244-pin, very low profile mini dual in-line memory module (VLP MiniDIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- 1GB (64 Meg x 72)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

Figure 1: 244-Pin VLP MiniDIMM



Options	Marking
• Register parity	P
• Package	
244-pin DIMM (lead-free)	Y
• Frequency/CAS latency[1]	
3ns @ CL = 5 (DDR2-667)	-667[2]
3.75ns @ CL = 4 (DDR2-533)	-53E
5.0ns @ CL = 3 (DDR2-400)	-40E
• PCB height	
0.72in. (18.3mm)	

Notes: 1. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.
2. Contact Micron for product availability.

Table 1: Address Table

	1GB
Refresh Count	8K
Row Addressing	16K (A0–A13)
Device Bank Addressing	4 (BA0, BA1)
Device Page Size per Bank	1KB
Device Configuration	512Mb (64 Meg x 8)
Column Addressing	1K (A0–A9)
Module Rank Addressing	2 (S0#, S1#)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4	CL = 5			
-667	–	533	667	15	15	55
-53E	400	533	–	15	15	55
-40E	400	400	–	15	15	55

Table 3: Part Numbers and Timing Parameters

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT18HVS12872(P)KY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT18HVS12872(P)KY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT18HVS12872(P)KY-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes: 1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HVS12872Y-40EC2.

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Pin Assignments and Descriptions

Table 4: Pin Assignments

244-Pin MiniDIMM Front								244-Pin MinDIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
1	VREF	32	VSS	63	VDDQ	94	DQS5#	123	VSS	154	DQ28	185	A3	216	NC/RDQS5#
2	VSS	33	DQ24	64	A2	95	DQS5	124	DQ4	155	DQ29	186	A1	217	VSS
3	DQ0	34	DQ25	65	VDD	96	VSS	125	DQ5	156	VSS	187	VDD	218	DQ46
4	DQ1	35	VSS	66	VSS	97	DQ42	126	VSS	157	DM3/RDQS3	188	CK0	219	DQ47
5	VSS	36	DQS3#	67	VSS	98	DQ43	127	DM0/RDQS0	158	NC/RDQS3#	189	CK0#	220	VSS
6	DQS0#	37	DQS3	68	PAR_IN/NC	99	VSS	128	NC/RDQS0#	159	VSS	190	VDD	221	DQ52
7	DQS0	38	VSS	69	VDD	100	DQ48	129	VSS	160	DQ30	191	A0	222	DQ53
8	VSS	39	DQ26	70	A10/AP	101	DQ49	130	DQ6	161	DQ31	192	BA1	223	VSS
9	DQ2	40	DQ27	71	BA0	102	VSS	131	DQ7	162	VSS	193	VDD	224	RFU
10	DQ3	41	VSS	72	VDD	103	SA2	132	VSS	163	CB4	194	RAS#	225	RFU
11	VSS	42	CB0	73	WE#	104	NC (Test)	133	DQ12	164	CB5	195	VDDQ	226	VSS
12	DQ8	43	CB1	74	VDDQ	105	VSS	134	DQ13	165	VSS	196	S0#	227	DM6/RDQS6
13	DQ9	44	VSS	75	CAS#	106	DQS6#	135	VSS	166	DM8/RDQS8	197	VDDQ	228	NC/RDQS6#
14	VSS	45	DQS8#	76	VDDQ	107	DQS6	136	DM1/RDQS1	167	NC//RDQS8#	198	ODT0	229	VSS
15	DQS1#	46	DQS8	77	S1#	108	VSS	137	NC/RDQS1#	168	VSS	199	A13	230	DQ54
16	DQS1	47	VSS	78	ODT1	109	DQ50	138	VSS	169	CB6	200	VDD	231	DQ55
17	VSS	48	CB2	79	VDDQ	110	DQ51	139	RFU	170	CB7	201	NC	232	VSS
18	Reset#	49	CB3	80	NC	111	VSS	140	RFU	171	VSS	202	VSS	233	DQ60
19	NC	50	VSS	81	VSS	112	DQ56	141	VSS	172	NC	203	DQ36	234	DQ61
20	VSS	51	NC	82	DQ32	113	DQ57	142	DQ14	173	VDDQ	204	DQ37	235	VSS
21	DQ10	52	VDDQ	83	DQ33	114	VSS	143	DQ15	174	CKE1	205	VSS	236	DM7/RDQS7
22	DQ11	53	CKE0	84	VSS	115	DQS7#	144	VSS	175	VDD	206	DM4/RDQS4	237	NC/RDQS7#
23	VSS	54	VDD	85	DQS4#	116	DQS7	145	DQ20	176	NC	207	NC/RDQS4#	238	VSS
24	DQ16	55	NC	86	DQS4	117	VSS	146	DQ21	177	NC	208	VSS	239	DQ62
25	DQ17	56	ERR_OUT/NC	87	VSS	118	DQ58	147	VSS	178	VDDQ	209	DQ38	240	DQ63
26	VSS	57	VDDQ	88	DQ34	119	DQ59	148	DM2/RDQS2	179	A12	210	DQ39	241	VSS
27	DQS2#	58	A11	89	DQ35	120	VSS	149	NC/RDQS2#	180	A9	211	VSS	242	SDA
28	DQS2	59	A7	90	VSS	121	SA0	150	VSS	181	VDD	212	DQ44	243	SCL
29	VSS	60	VDD	91	DQ40	122	SA1	151	DQ22	182	A8	213	DQ45	244	VDDSPD
30	DQ18	61	A5	92	DQ41			152	DQ23	183	A6	214	VSS		
31	DQ19	62	A4	93	VSS			153	VSS	184	VDDQ	215	DM5/RDQS5		

Note: Pins 56 and 68 are only used for parity registers; both are NC for non-parity modules.

Figure 2: Pin Locations

Very Low Profile

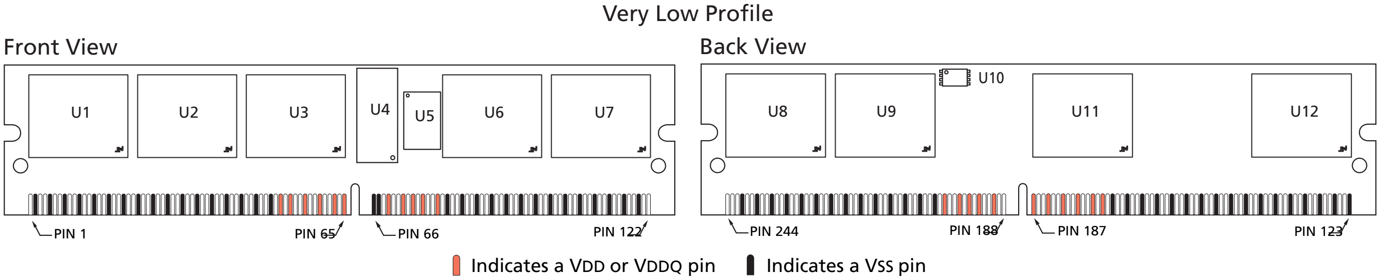


Table 5: Pin Descriptions
Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
78, 198	ODT0, ODT1	Input	On-Die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, RDQS, RDQS#, CB, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
188, 189	CK0, CK0#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
53, 174	CKE0, CKE1	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all device banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any device bank). CKE is synchronous for POWER-DOWN entry, POWER-DOWN exit, output disable, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh operation V_{REF} must be maintained to this input.
77, 196	S0#, S1#	Input	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
73, 75, 194	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
71, 192	BA0, BA1	Input	Bank address inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.
58, 59, 61, 62, 64, 70, 179, 180, 182, 183, 185, 186, 191, 199	A0–A13	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for Read/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.

Table 5: Pin Descriptions
Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
3, 4, 9, 10, 12, 13, 21, 22, 24, 25, 30, 31, 33, 34, 39, 40, 82, 83, 88, 89, 91, 92, 97, 98, 100, 101, 109, 110, 112, 113, 118, 119, 124, 125, 130, 131, 133, 134, 142, 143, 145, 146, 151, 152, 154, 155, 160, 161, 203, 204, 209, 210, 212, 213, 218, 219, 221, 222, 230, 231, 233, 234, 239, 240	DQ0–DQ63	I/O	Data input/output: Bidirectional data bus.
6, 7, 15, 16, 27, 28, 36, 37, 45, 46, 85, 86, 94, 95, 106, 107, 115, 116	DQS0–DQS8	I/O	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
127, 136, 148, 157, 166, 206, 215, 227, 236	DM0/RDQS0–DM8/RDQS8	I/O	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. If RDQS is disabled, RDQS0–RDQS8 function only as DM0–DM8 and RDQS0#–RDQS8# are not used (NC).
128, 137, 149, 158, 167, 207, 216, 228, 237	RDQS0#–RDQS8#	I/O	Redundant DQS: If RDQS is disabled, RDQS0–RDQS8 become DM0–DM8 only and RDQS0#–RDQS8# are not used (NC).
42, 43, 48, 49, 163, 164, 169, 170	CB0–CB7	I/O	Check bits.
68 (NC for non-parity)	PAR_IN	Input	Parity bit for the address and control bus.
56 (NC for non-parity)	ERR_OUT	Output	Parity error found on the address and control bus.
243	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
103, 121, 122	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
242	SDA	I/O	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
18	Reset#	Input	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.
54, 60, 65, 69, 72, 175, 181, 187, 190, 193, 200	VDD	Supply	Power supply: 1.8V ±0.1V.
52, 57, 63, 74, 76, 79, 173, 178, 184, 195, 197	VDDQ	Supply	DQ power supply: 1.8V ±0.1V.
1	VREF	Supply	SSTL_18 reference voltage.

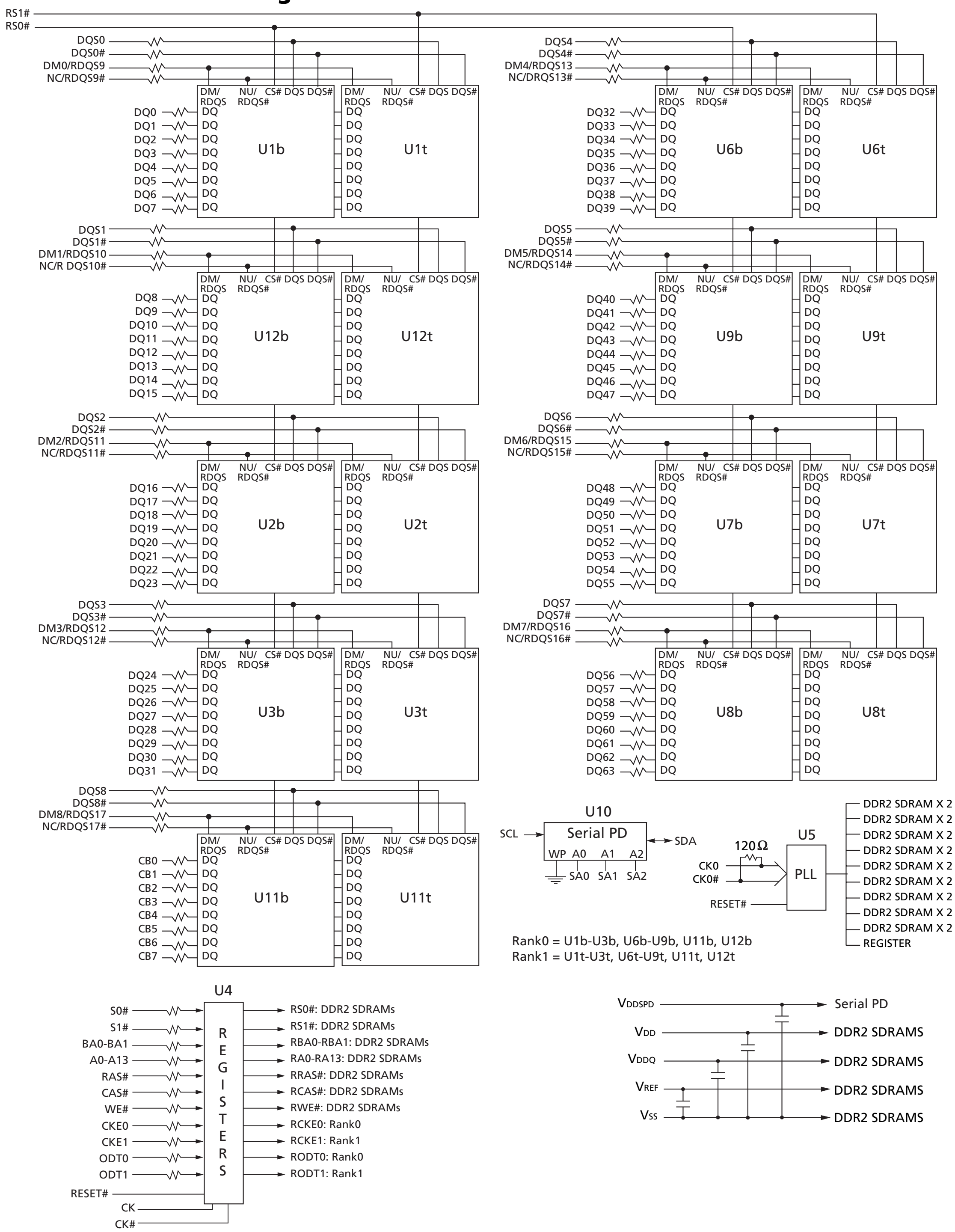
Table 5: Pin Descriptions
Pin numbers may not correlate with symbols; refer to Pin Assignment tables on page 6 for more information

Pin Numbers	Symbol	Type	Description
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 66, 67, 81, 84, 87, 90, 93, 96, 99, 102, 105, 108, 111, 114, 117, 120, 123, 126, 129, 132, 135, 138, 141, 144, 147, 150, 153, 156, 159, 162, 165, 168, 171, 202, 205, 208, 211, 214, 217, 220, 223, 226, 229, 232, 235, 238, 241	V_{SS}	Supply	Ground.
244	V_{DDSPD}	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
19, 51, 55, 80, 104, 128, 137, 149, 158, 167, 172, 176, 177, 201, 207, 216, 228, 237	NC	–	No connect: These pins should be left unconnected.
139, 140, 224, 225	RFU	–	Reserved for future use.

Functional Block Diagram

Unless otherwise noted, resistor values are 22Ω. Micron module part numbers are explained in the Module Part Numbering Guide at www.micron.com/support/numbering.html. Modules use the following DDR2 SDRAM devices: MT47H64M8BT. Component specifications are available at: www.micron.com/products/ddr2sdram.

Figure 3: Functional Block Diagram



General Description

The MT18HVS12872(P)K DDR2 SDRAM module is a high-speed, CMOS, dynamic random-access 1GB memory module organized in x72 configuration. DDR2 SDRAM modules use internally configured quad-bank DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

PLL and Register Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum DC Ratings

Symbol	Parameter		Min	Max	Units
VDD	VDD Supply Voltage Relative to VSS		-1.0	2.3	V
VDDQ	VDDQ Supply Voltage Relative to VSS		-0.5	2.3	V
VDDL	VDDL Supply Voltage Relative to Vss		-0.5	2.3	V
VIN, VOUT	Voltage on any Pin Relative to VSS		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	°C
T_{case}	DDR2 SDRAM Device Operating Temperature (Ambient)		0	85	°C
T_{OPR}	Operating Temperature (Ambient)		0	55	°C
I_I	Input Leakage Current; Any input 0V ≤ VIN ≤ VDD; VREF input 0V ≤ VIN ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE, CK, CK#, DM	-5	5	µA
I_{OZ}	Output Leakage Current; 0V ≤ VOUT ≤ VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	VREF Leakage Current; VREF = Valid VREF level		-18	18	µA

Capacitance

At DDR2 data rates, Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

Table 7: IDD Specifications and Conditions – 1GB
Values shown for DDR2 SDRAM components only

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current; $^tCK = {}^tCK$ (IDD), $^tRC = {}^tRC$ (IDD), $^tRAS = {}^tRAS$ MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD0	855	765	765	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $^tCK = {}^tCK$ (IDD), $^tRC = {}^tRC$ (IDD), $^tRAS = {}^tRAS$ MIN (IDD), $^tRCD = {}^tRCD$ (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1	990	900	855	mA
Precharge power-down current; All device banks idle; $^tCK = {}^tCK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2P	90	90	90	mA
Precharge quiet standby current; All device banks idle; $^tCK = {}^tCK$ (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		IDD2Q	900	720	630	mA
Precharge standby current; All device banks idle; $^tCK = {}^tCK$ (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD2N	990	810	720	mA
Active power-down current; All device banks open; $^tCK = {}^tCK$ (IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	IDD3P	630	540	450	mA
	Slow PDN Exit MR[12] = 1		180	180	180	mA
Active standby current; All device banks open; $^tCK = {}^tCK$(IDD), $^tRAS = {}^tRAS$ MAX (IDD), $^tRP = {}^tRP$(IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N	1,170	990	810	mA
Operating burst write current; All device banks open, Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $^tCK = {}^tCK$ (IDD), $^tRAS = {}^tRAS$ MAX (IDD), $^tRP = {}^tRP$ (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4W	1,440	1,215	1,035	mA
Operating burst read current; All device banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; $^tCK = {}^tCK$ (IDD), $^tRAS = {}^tRAS$ MAX (IDD), $^tRP = {}^tRP$ (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD4R	1,620	1,350	1,080	mA
Burst refresh current; $^tCK = {}^tCK$ (IDD); Refresh command at every ^tRFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5	3,780	3,600	3,420	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		IDD6	90	90	90	mA
Operating bank interleave read current; All device banks interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = ^tRCD (IDD)-1 x ^tCK (IDD); $^tCK = {}^tCK$ (IDD), $^tRC = {}^tRC$(IDD), $^tRRD = {}^tRRD$(IDD), $^tRCD = {}^tRCD$(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING; See IDD7 Conditions for detail.		IDD7	2,565	2,385	2,115	mA

AC Operating Specifications

Recommended AC operating conditions are given in the DDR2 component data sheets, available at www.micron.com/products/ddr2sdram. Module speed grades correlate with component speed grades as shown in the following table:

Table 8: Module and Component Speed Grade Table

Module Speed Grade	Component Speed Grade
-80E	-25E
-667	-3
-53E	-37E
-40E	-5E

PLL and Register Specifications

Table 9: Register Timing Requirements and Switching Characteristics

Symbol	Parameter	Condition	0°C ≤ T_{OPR} ≤ +55°C VDD = +1.8V ±0.1V		Units
			Min	Max	
VOH		IOH = -6 mA	1.2	–	V
VOL		IOL = 6 mA	–	.05	V
II	All Inputs	VI = VDD or GND	–	5	µA
IDD	Static Standby	RESET# = GND	–	100	µA
	Static Operating	RESET# = VDD, VI = VIH(AC) or VIL(AC), I_0 = 0	–	40	mA
IDDD	Dynamic Operating – Clock Only	RESET# = VDD, VI = VIH(AC) or VIL(AC), I_0 = 0; CK and CK# switching 50% duty cycle	Varies by Mfr	Varies by Mfr	µA
	Dynamic Operating – per each data input, 1:1 mode	RESET# = VDD, VI = VIH(AC) or VIL(AC), I_0 = 0; CK and CK# switching 50% duty cycle; one data input switching at ^{t}CK/2, 50% duty cycle	Varies by Mfr	Varies by Mfr	
	Dynamic Operating – per each data input, 1:2 mode	RESET# = VDD, VI = VIH(AC) or VIL(AC), I_0 = 0; CK and CK# switching 50% duty cycle; one data input switching at ^{t}CK/2, 50% duty cycle	Varies by Mfr	Varies by Mfr	
CI	Data Inputs	VI = VREF ±250mV	2.5	3.5	pF
	CK and CK#	VICR = 0.9V, VID = 600mV	2	3	
	RESET	VI = VDD or GND	Varies	Varies	

Table 10: Register Electrical Characteristics
Note: 1

Register	Symbol	Parameter	Condition	0°C ≤ T_{OPR} ≤ +55°C VDD = +1.8V ±0.1V		Units	Notes
				Min	Max		
SSTL (bit pattern by JESD82)	f_{clock}	Clock Frequency		–	270	MHz	
	t_w	Pulse Duration		1	–	ns	
	t_{act}	Differential Inputs Active Time		–	10	ns	2, 3
	t_{inact}	Differential Inputs Inactive Time		–	15	ns	2, 4
	t_{su}	Setup Time	Data Before CK HIGH, CK# LOW	0.7	–	ns	
			Data Before CK HIGH, CK# LOW	0.5	–	ns	
			ODT, CKE, and Data before CK HIGH, CK# LOW	0.5	–		
	t_h	Hold Time	OKE, CKE, and Data after CK HIGH, CK# LOW	0.50	–	ns	

Notes:
1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC Standard JESD82.
2. This parameter is not necessarily production tested.
3. Data inputs must be low a minimum time of t_{act} (MAX), after RESET# is taken HIGH.
4. Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} (MAX), after RESET# is taken LOW.

Table 11: PLL Clock Driver Electrical Characteristics

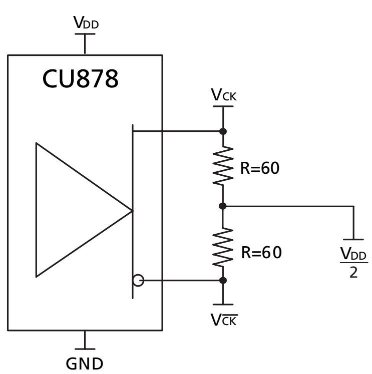
Symbol	Parameter	Test Condition	0°C ≤ T_{OPR} ≤ +55°C V_{DD} = +1.8V ±0.1V Min	Nominal	Max	Units	Notes
V_{IK}	All inputs	I_I = -18mA	–	–	-1.2	V	
V_{OH}	High output voltage	I_{OH} = -100µA	V_{DDQ}/2 - 0.2	–	–	V	
		I_{OH} = -9mA	1.1	–	–	V	
V_{OL}	Low output voltage	I_{OL} = 100µA		–	0.1	µA	
		I_{OL} = 9mA			0.6	V	
I_{ODL}	Output disabled low current	OE = L, V_{ODL} = 100mV	100	–	–	µA	
V_{OD}	Output differential voltage, the magnitude of the difference between the true and complimentary outputs		0.6	–	–	V	
I_I	CK, CK#	V_I = V_{DDQ} or GND	–	–	±250	µA	
I_{DDLD}	Static supply current: I_{DDQ} + I_{ADD}	CK and CK# = L	–	–	500	µA	
I_{DD}	Dynamic supply current: I_{DDQ} + I_{ADD}	CK and CK# = 270 MHz, all outputs are open (not connected to a PCB)	–	–	300	mA	1
C_I	CI and CK#	V_I = V_{DDQ} or GND	2	–	3	pF	
$C_{I(\Delta)}$	CI and CK#	V_I = V_{DDQ} or GND	V_{DDQ}/2 - 0.2	–	0.25	pF	

Notes: 1. Total I_{DD} = I_{DDQ} = I_{ADD} = F_{CK} x C_{PD} x V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} x V_{DDQ}) where F_{CK} is the input frequency, V_{DDQ} is the power supply and C_{PD} is the power dissipation capacitance.

Table 12: PLL Clock Driver Timing Requirements and Switching Characteristics
Note: 1

Parameter	Symbol	0°C ≤ T_{OPR} ≤ +55°C VDD = +1.8V ±0.1V			Units	Notes
		Min	Nominal	Max		
Output Enable to any Y/Y#	^{t}EN	–	–	8	ns	
Output Enable to any Y/Y#	^{t}DIS	–	–	8	ns	
Cycle to Cycle Jitter	$^{t}JIT_{CC}$	-40	–	40	ps	
Static Phase Offset	$^{t}\varnothing$	-50	0	50	ps	2
Dynamic Phase Offset	$^{t}\varnothing_{dyn}$	-50	0	50	ps	2
Output Clock Skew	$^{t}SK_{O}$	–	–	40	ps	
Period Jitter	$^{t}JIT_{PER}$	-40	–	40	ps	3, 4
Half-Period Jitter	$^{t}JIT_{HPER}$	-75	–	75	ps	3
Input Clock Slew Rate	$^{t}LS_{I}$	1.0	2.5	4	V/ns	
Output Clock Slew Rate	$^{t}LS_{O}$	1.5	2.5	3	V/ns	6
Output Differential-Pair Cross-Voltage	VOX	VDDQ/2 - 0.1	–	VDDQ/2 + 0.1	V	5
SSC Modulation Frequency		30	–	33	kHZ	
SSC Clock Input Frequency Deviation		0.0	–	-0.50	%	
PLL Loop Bandwidth (-3dB from unity gain)		2.0	–	–	MHz	

Notes:
1. Timing and switching specifications for the PLL listed above are critical for proper operation of the DDR2 SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this PLL is available in JEDEC Standard JESD82.
2. Static Phase Offset does not include Jitter.
3. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
4. Design target is 60ps, unless it is unachievable.
5. VOX specified at the DRAM clock input, or the test load.
6. The Output Slew Rate is determined from the IBIS model:



Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figure 4 on page 18, and Figure 5 on page 19).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 6 on page 19).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 4: Data Validity

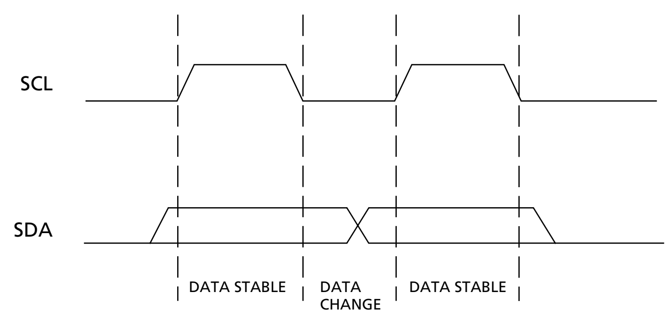


Figure 5: Definition of Start and Stop

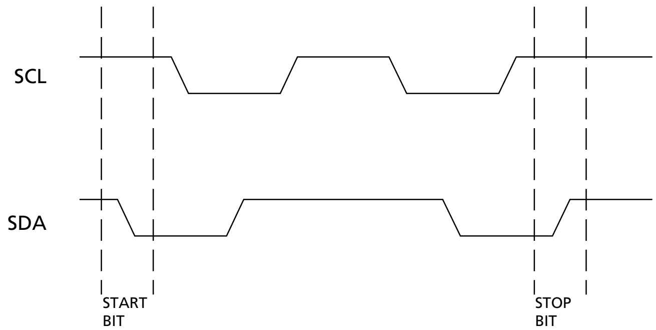


Figure 6: Acknowledge Response From Receiver

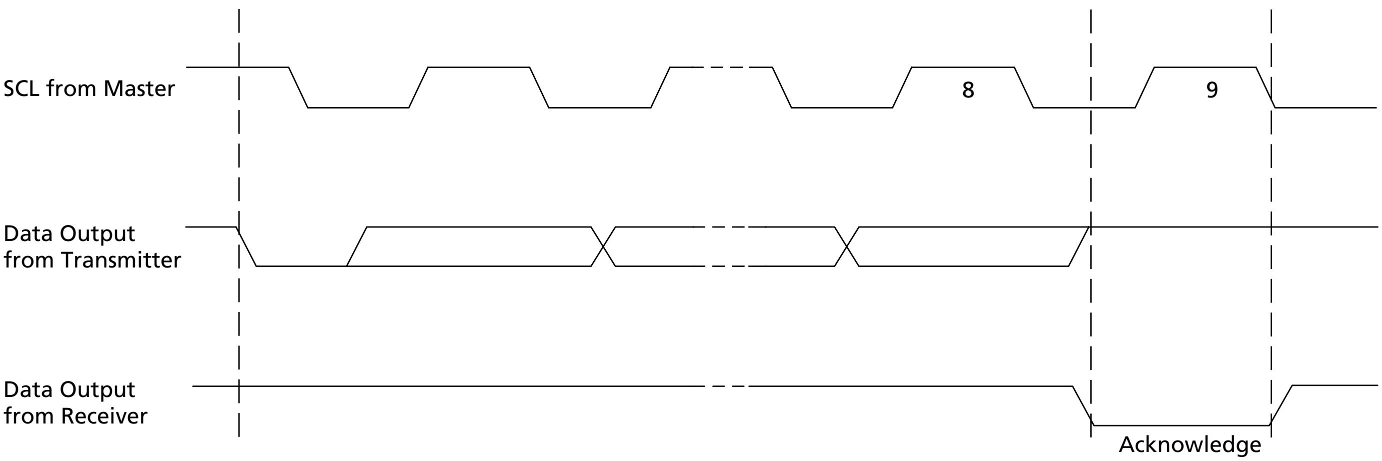


Table 13: EEPROM Device Select Code
The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			R$\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	R$\overline{W}$
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	R$\overline{W}$

Table 14: EEPROM Operating Modes

Mode	R$\overline{W}$ Bit	$\overline{WC}$	Bytes	Initial Sequence
Current Address Read	1	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	0	V_{IH} or V_{IL}	1	START, Device Select, R$\overline{W}$ = '0', Address
	1	V_{IH} or V_{IL}	1	reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	1	V_{IH} or V_{IL}	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{W}$ = '0'
Page Write	0	V_{IL}	≤ 16	START, Device Select, R$\overline{W}$ = '0'

Figure 7: SPD EEPROM Timing Diagram

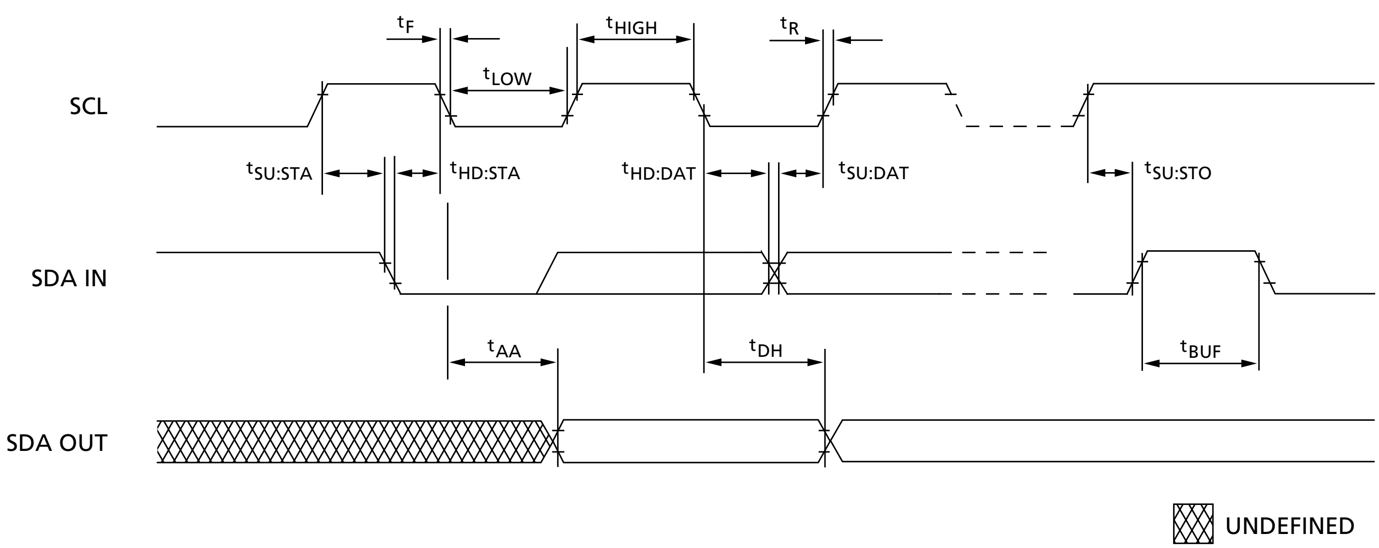


Table 15: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply Voltage	V_{DDSPD}	1.7	3.6	V
Input High Voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 0.5	V
Input Low Voltage: Logic 0; All inputs	V_{IL}	-0.6	V_{DDSPD} x 0.3	V
Output Low Voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input Leakage Current: V_{IN} = GND to V_{DDSPD}	I_{LI}	0.10	3	µA
Output Leakage Current: V_{OUT} = GND to V_{DDSPD}	I_{LO}	0.05	3	µA
Standby Current:	I_{SB}	1.6	4	µA
Power Supply Current, READ: SCL clock frequency = 100 KHz	I_{CC_R}	0.4	1	mA
Power Supply Current, WRITE: SCL clock frequency = 100 KHz	I_{CC_W}	2	3	mA

Table 16: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3		µs	
Data-out hold time	^tDH	200		ns	
SDA and SCL fall time	^tF		300	ns	2
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	0.6		µs	
Clock HIGH period	^tHIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR		0.3	µs	2
SCL clock frequency	^tSCL		400	KHz	
Data-in setup time	$^tSU:DAT$	100		ns	
Start condition setup time	$^tSU:STA$	0.6		µs	3
Stop condition setup time	$^tSU:STO$	0.6		µs	
Write cycle time	^tWRC		10	ms	4

Notes:
1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a write cycle.
4. The SPD EEPROM write cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the write cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 17: Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 23

Byte	Description	Entry (Version)	MT9HVF6472K/ MT18HVS12872(P)K
0	Number of SPD Bytes Used by Micron	128	80
1	Total Number of Bytes in SPD Device	256	08
2	Fundamental Memory Type	DDR2 SDRAM	08
3	Number of Row Addresses on Assembly	13	0E
4	Number of Column Addresses on Assembly	10	0A
5	DIMM Height and Module Ranks	0.72in., Dual Rank	11
6	Module Data Width	72	48
7	Module Data Width (Continued)	0	00
8	Module Voltage Interface Levels	SSTL 1.8V	05
9	SDRAM Cycle Time, ^{t}CK (CL = Maximum value, see byte 18)	-667 -53E -40E	30 3D 50
10	SDRAM Access from Clock,^{t}AC (CL = Maximum value, see byte 18)	-667 -53E -40E	45 50 60
11	Module Configuration Type	ECC/ECC and parity	02/06
12	Refresh Rate/Type	7.81µs/SELF	82
13	SDRAM Device Width (Primary SDRAM)	8	08
14	Error-checking SDRAM Data Width	8	08
15	Minimum Clock Delay, Back-to-Back Random Column Access	1 clock	00
16	Burst Lengths Supported	4, 8	0C
17	Number of Banks on SDRAM Device	4 or 8	04
18	CAS Latencies Supported	-667 (5, 4, 3) -53E/-40E (4, 3)	38 18
19	Module Thickness		03
20	DDR2 DIMM Type	Reg. MiniDIMM	10
21	SDRAM Module Attributes		04
22	SDRAM Device Attributes: Weak Driver (01) and 50Ω ODT (03)	-667 -53E/-40E	03 01
23	SDRAM Cycle Time, ^{t}CK, Max. CL - 1	-667 -53E/-40E	3D 50
24	SDRAM Access from CK, ^{t}AC, Max. CL - 1	-667 -53E -40E	45 50 60
25	SDRAM Cycle Time, ^{t}CK, Max. CL - 2	-667 -53E/-40E(N/A)	50 00
26	SDRAM Access from CK, ^{t}AC, Max. CL - 2	-667 -53E/-40E(N/A)	45 00
27	Minimum Row Precharge Time, ^{t}RP		3C
28	Minimum Row Active to Row Active, ^{t}RRD		1E
29	Minimum RAS# to CAS# Delay, ^{t}RCD		3C
30	Minimum RAS# Pulse Width, ^{t}RAS (see note 1)	-667/-53E -40E	2D 28
31	Module Rank Density	512MB	80

Table 17: Serial Presence-Detect Matrix
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"; table notes located on page 23

Byte	Description	Entry (Version)	MT9HVF6472K/ MT18HVS12872(P)K
32	Address and Command Setup Time, ^tIS_b	-667 -53E -40E	20 25 35
33	Address and Command Hold Time, ^tIH_b	-667 -53E -40E	27 37 47
34	Data/ Data Mask Input Setup Time, ^tDS_b	-667/-53E -40E	10 15
35	Data/ Data Mask Input Hold Time, ^tDH_b	-667 -53E -40E	17 22 27
36	Write Recovery Time, ^tWR		3C
37	Write to Read CMD Delay, ^tWTR	-667/-53E -40E	1E 28
38	Read to Precharge CMD Delay, ^tRTP		1E
39	Mem Analysis Probe		00
40	Extension for bytes 41 and 42		00
41	Min Active Auto Refresh Time, ^tRC	-667/-53E -40E	3C 37
42	Minimum Auto Refresh to Active/ Auto Refresh Command Period, ^tRFC		69
43	SDRAM Device Max Cycle Time, $^tCK_{MAX}$		80
44	SDRAM Device Max DQS-DQ Skew Time, ^tDQSQ	-667 -53E -40E	18 1E 23
45	SDRAM Device Max Read Data Hold Skew Factor, ^tQHS	-667 -53E -40E	22 28 2D
46	PLL Relock Time		0F
47–61	Optional features, not supported		00
62	SPD Revision	Release 1.2	12
63	Checksum For Bytes 0–62 ECC/ECC and Parity	-667 -53E -40E	31/35 DC/E0 43/47
64	Manufacturer's JEDEC ID Code	MICRON	2C
65–71	Manufacturer's JEDEC ID Code	(Continued)	FF
72	Manufacturing Location	01–12	01–0C
73–90	Module Part Number (ASCII)		Variable Data
91	PCB Identification Code	1–9	01–09
92	Identification Code (Continued)	0	00
93	Year of Manufacture in BCD		Variable Data
94	Week of Manufacture in BCD		Variable Data
95–98	Module Serial Number		Variable Data
99–127	Manufacturer-Specific Data (RSVD)		–

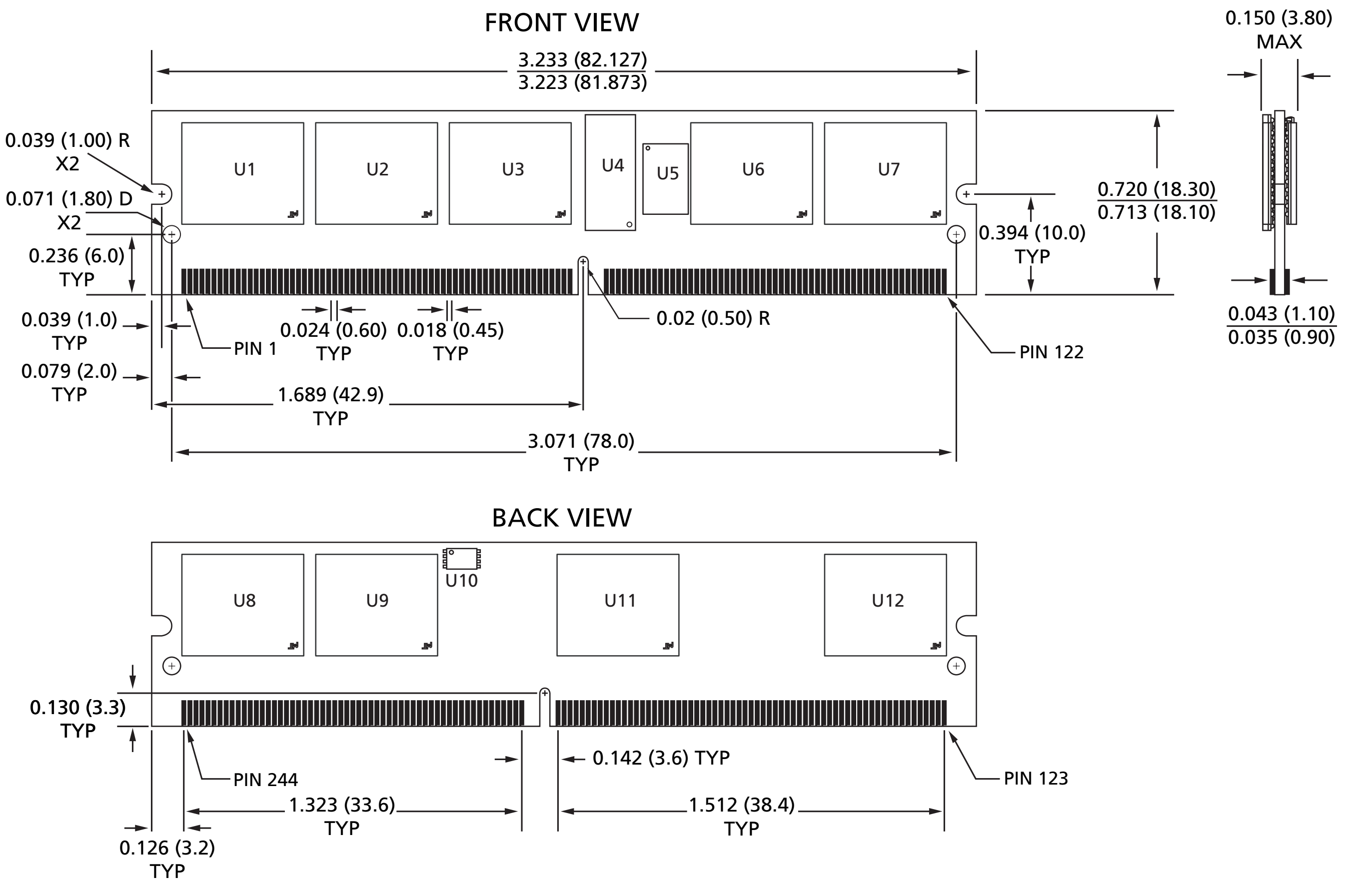
Notes: 1. The ^tRAS SPD value shown is based on the JEDEC standard value of 45 ns; the actual device specification is ^tRAS = 40ns.

Package Dimensions

All dimensions are in inches (millimeters); $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

Figure 8: 244-Pin VLP Registered MiniDIMM Dimensions



Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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