



Micron PISMO[™] Module Data Sheet

PISMO2-00021: Mobile DDR DRAM + 1.8V/3.3V NAND Flash

Introduction

The PISMO (Platform Independent Storage MOdule) specification provides a standard external interface to ease memory performance evaluation. This document describes the mechanical and functional features, configuration options, and design specifications of a Micron PISMO2-compliant module. This small, stackable module features a combination of Mobile DRAM and NAND Flash memory, as described in Table 1. The board includes:

- three memory chip footprints (only two are in use at once)
- the bottom connector to the host system (J2)
- the top connector (J1, for stacking multiple boards)
- a 64Kb serial EEPROM for configuration and presence detection
- a 3.3V power generation circuit based on a Linear Technology DC-DC converter

PISMO2-00021 options and part markings are described in Figure 12 on page 21. Reference documents and data sheets are listed in Table 10 on page 21.

Micron PISMO2-00021 Features

Physical Module Mechanics

- Stackable memory module (up to four active modules)
- Plain rectangular PCB (60mm x 50mm)
- Stacking height: 7mm (other stacking heights will become available later)
- Supports additional debugging tools (for example, a logic analyzer adapter)
- Supports spacers with or without screw option

Supported Memory Interfaces

- Dynamic memory: 128Mb to 1Gb; x32; 1.8V Micron Mobile DDR SDRAM MT46HxxM32LF – 1/2/4/8 Meg x 32 x 4 banks
- NAND memory: 1Gb–16Gb; x8 or x16; 1.8V/3.3V; 48-pin TSOP NAND Flash memory
- Serial EEPROM for presence detection: 64Kb

Table 1: PISMO2-00021 Module Memory Technologies

| Technology | Density | Voltage | Data Bus | Package |
|------------------|-----------|-----------|---------------------------|--------------------------|
| Mobile DDR SDRAM | 128Mb–1Gb | 1.8V | 32-bit | 90-ball VFPGA |
| NAND Flash | 1Gb–16Gb | 1.8V/3.3V | 8- or 16-bit, multiplexed | 48-pin TSOP (SLC or MLC) |



PISMO2-00021: Micron Mobile DRAM + NAND Module Pin Assignments and Descriptions

Table 2: Supported NAND Flash Device Characteristics

| Supported Device | Die | Bus Width | Density | Technology | Voltage |
|------------------|------|-----------|---------|------------|-----------|
| MT29F4G08AAA | M40A | x8 | 4Gb | SLC | 3.3V |
| MT29F8G08DAA | M40A | x8 | 8Gb | SLC | 3.3V |
| MT29F16G08FAA | M40A | x8 | 16Gb | SLC | 3.3V |
| MT29F2GxxAACWP | M49A | x8/x16 | 2Gb | SLC | 1.8V/3.3V |
| MT29F4GxxBACWP | M49A | x8/x16 | 4Gb | SLC | 1.8V/3.3V |
| MT29F8GxxFACWP | M49A | x8/x16 | 8Gb | SLC | 1.8V/3.3V |
| MT29F8G08MAAWC | L41B | x8 | 8Gb | MLC | 3.3V |
| MT29F16G08QAAWC | L41B | x8 | 16Gb | MLC | 3.3V |
| MT29F32G08TAAWC | L41B | x8 | 32Gb | MLC | 3.3V |
| MT29F8G16MAAWC | L41B | x16 | 8Gb | MLC | 3.3V |
| MT29F16G16QAAWC | L41B | x16 | 16Gb | MLC | 3.3V |
| MT29F32G16TAAWC | L41B | x16 | 32Gb | MLC | 3.3V |

Pin Assignments and Descriptions

The meanings of the signal name prefixes are explained in Table 3. Tables 4 and 5 illustrate the signal locations within the bottom and top PISMO2-00021 connectors, respectively.

Table 3: Naming Conventions for PISMO2 Specification Signals

| Signal Prefix | Definition |
|---------------|--|
| SM | The "SM_" prefix identifies PISMO2 static memory interface signals. This interface supports NOR Flash, DiskOnChip, SRAM and PSRAM memory, and memory-mapped I/O devices. |
| DM | The "DM_" prefix identifies PISMO2 dynamic memory interface signals. This interface supports SDR or DDR SDRAM memory. |
| NA | The "NA_" prefix identifies PISMO2 NAND Flash memory interface signals. This interface supports NAND Flash memory. |
| FS | The "FS_" prefix identifies PISMO2 serial memory interface signals. This interface supports serial Flash memory or I/O devices with a serial bus interface. |
| AUX | The "AUX_" prefix identifies PISMO2 module management interface signals. This interface supports hardware production and testing, module control functions, and plug-and-play enumeration. |



PISMO2-00021: Micron Mobile DRAM + NAND Module Pin Assignments and Descriptions

Table 4: PISMO2-00021 Bottom Connector (J2) Pin Assignments

| Col. | Row A | Row B | Row C | Row D | Row E | Row F | Row G | Row H |
|------|------------|------------|------------|------------|------------|------------|------------|---------------|
| 1 | DM_DQS3_DH | DM_DQS3_DL | DNU11 | DM_CS1_N | Vss46 | FS_SCK | FS_SO | FS_RESET_N |
| 2 | DM_D26 | DM_D24 | DM_BA2 | DM_A15 | DM_A4 | Vss45 | FS_SI | FS_HOLD_N |
| 3 | DM_D27 | DM_D25 | DM_RESET_N | DM_A7 | DM_A6 | FS_V33_0 | DNU9 | FS_CS3_N |
| 4 | DM_D29 | DM_D28 | DM_ODT1 | DM_A11 | DM_A9 | Vss44 | FS_VIO_1 | FS_CS2_N |
| 5 | DM_D30 | DM_D31 | DM_ODT0 | DM_CKE1 | DM_CKE0 | Vss43 | FS_VIO_0 | FS_CS1_N |
| 6 | DM_DQS1_DH | DM_DQS1_DL | DM_VREF | DM_A14 | DM_DQM3 | Vss42 | FS_V18_0 | FS_CS0_N |
| 7 | DM_D8 | DM_D9 | DM_VIO_9 | DM_A8 | DM_A12 | Vss41 | FS_WP_N | AUX_SA2 |
| 8 | DM_D10 | DM_D11 | DM_VIO_3 | DM_DQM1 | DM_A5 | Vss40 | AUX_SCL | AUX_SA1 |
| 9 | DM_D12 | DM_D13 | DM_VIO_6 | Vss37 | Vss38 | Vss39 | AUX_SDA | AUX_SA0 |
| 10 | DM_D15 | DM_D14 | DM_VIO_5 | DM_CLK1_DH | DM_CLK1_DL | Vss36 | AUX_TDI | AUX_TDO |
| 11 | DM_D1 | DM_D0 | DM_VIO_8 | Vss34 | Vss35 | AUX_V33_1 | AUX_TCK | AUX_TMS |
| 12 | DM_D3 | DM_D2 | DM_VIO_4 | DM_CLK0_DH | DM_CLK0_DL | Vss33 | DNU13 | AUX_PRESENT_N |
| 13 | DM_D5 | DM_D4 | DM_VCC_3 | Vss31 | Vss32 | AUX_V33_0 | AUX_POR_N | AUX_HMR_N |
| 14 | DM_D6 | DM_D7 | DM_VIO_2 | DM_A10 | DM_A2 | Vss30 | AUX_V33_2 | AUX_STANDBY_N |
| 15 | DM_DQS0_DH | DM_DQS0_DL | DM_VIO_7 | DM_WE_N | DM_CS0_N | Vss29 | DNU7 | DNU8 |
| 16 | DM_D16 | DM_D17 | DM_VCC_2 | DM_DQM0 | DM_A13 | NA_VIO_2 | NA_IO15 | NA_IO7 |
| 17 | DM_D19 | DM_D18 | DM_VCC_1 | DM_RAS_N | DM_CAS_N | Vss28 | NA_IO14 | NA_IO6 |
| 18 | DM_D22 | DM_D20 | DM_VIO_1 | DM_BA1 | DM_BA0 | Vss27 | NA_IO13 | NA_IO5 |
| 19 | DM_D23 | DM_D21 | DM_VIO_0 | DM_A1 | DM_A0 | Vss26 | NA_IO12 | NA_IO4 |
| 20 | DM_DQS2_DH | DM_DQS2_DL | DM_VCC_0 | DM_DQM2 | DM_A3 | Vss25 | NA_IO11 | NA_IO3 |
| 21 | Vss20 | Vss21 | Vss22 | Vss23 | Vss24 | NA_VIO_1 | NA_IO10 | NA_IO2 |
| 22 | SM_D23 | SM_D31 | SM_V33_2 | SM_A30 | SM_A31 | Vss19 | NA_IO9 | NA_IO1 |
| 23 | SM_D22 | SM_D30 | SM_V33_1 | SM_A28 | SM_A29 | Vss18 | NA_IO8 | NA_IO0 |
| 24 | SM_D21 | SM_D29 | SM_V33_0 | SM_A26 | SM_A27 | Vss17 | DNU12 | NA_PRE |
| 25 | SM_D20 | SM_D28 | SM_VIO_8 | SM_A24 | SM_A25 | Vss16 | NA_RY | NA_RE_N |
| 26 | SM_D19 | SM_D27 | SM_VIO_7 | SM_A22 | SM_A23 | NA_VIO_0 | NA_CS2_N | NA_CS3_N |
| 27 | SM_D18 | SM_D26 | SM_VIO_6 | SM_A20 | SM_A21 | NA_V33_0 | NA_CS1_N | NA_CS0_N |
| 28 | SM_D17 | SM_D25 | SM_VIO_5 | SM_A18 | SM_A19 | NA_V18_0 | NA_CLE | NA_ALE |
| 29 | SM_D16 | SM_D24 | SM_CLK3 | SM_A16 | SM_A17 | Vss15 | NA_WE_N | NA_WP_N |
| 30 | DNU16 | Vss12 | SM_CLK2 | Vss13 | SM_BE2 | Vss14 | DNU5 | DNU6 |
| 31 | DNU17 | Vss9 | SM_CLK1 | Vss10 | SM_BE3 | SM_OE_N | Vss11 | DNU4 |
| 32 | SM_D7 | SM_D15 | SM_CLK0 | SM_A14 | SM_A15 | SM_WE_N | Vss8 | DNU3 |
| 33 | SM_D6 | SM_D14 | SM_VIO_4 | SM_A12 | SM_A13 | SM_LBA_N | Vss7 | SM_WP_N |
| 34 | SM_D5 | SM_D13 | SM_VIO_3 | SM_A10 | SM_A11 | SM_BUSY_N | Vss6 | SM_RESET_N |
| 35 | SM_D4 | SM_D12 | SM_VIO_2 | SM_A8 | SM_A9 | SM_BWAIT_N | Vss5 | SM_PD |
| 36 | SM_D3 | SM_D11 | SM_VIO_1 | SM_A6 | SM_A7 | Vss4 | DNU1 | DNU2 |
| 37 | SM_D2 | SM_D10 | SM_VIO_0 | SM_A4 | SM_A5 | Vss3 | SM_IRQ_N | SM_CS3_N |
| 38 | SM_D1 | SM_D9 | SM_V18_2 | SM_A2 | SM_A3 | Vss2 | SM_CRE | SM_CS2_N |
| 39 | SM_D0 | SM_D8 | SM_V18_1 | SM_A0 | SM_A1 | Vss1 | SM_DMARQ_N | SM_CS1_N |
| 40 | DNU14 | DNU15 | SM_V18_0 | SM_BE0 | SM_BE1 | Vss0 | DNU0 | SM_CS0_N |



PISMO2-00021: Micron Mobile DRAM + NAND Module Pin Assignments and Descriptions

Table 5: PISMO2-00021 Top Connector (J1) Pin Assignments

| Col. | Row A | Row B | Row C | Row D | Row E | Row F | Row G | Row H |
|------|------------|------------|------------|------------|------------|------------|------------|---------------|
| 1 | DM_DQS3_DH | DM_DQS3_DL | DNU11 | DM_VIO | Vss46 | FS_SCK | FS_SO | FS_RESET_N |
| 2 | DM_D26 | DM_D24 | DM_BA2 | DM_A15 | DM_A4 | Vss45 | FS_SI | FS_HOLD_N |
| 3 | DM_D27 | DM_D25 | DM_RESET_N | DM_A7 | DM_A6 | FS_V33_0 | DNU9 | FS_CS3_N |
| 4 | DM_D29 | DM_D28 | DM_ODT1 | DM_A11 | DM_A9 | Vss44 | FS_VIO_1 | FS_CS2_N |
| 5 | DM_D30 | DM_D31 | DM_ODT0 | DM_CKE1 | DM_CKE0 | Vss43 | FS_VIO_0 | FS_CS1_N |
| 6 | DM_DQS1_DH | DM_DQS1_DL | DM_VREF | DM_A14 | DM_DQM3 | Vss42 | FS_V18_0 | FS_CS0_N |
| 7 | DM_D8 | DM_D9 | DM_VIO_9 | DM_A8 | DM_A12 | Vss41 | FS_WP_N | AUX_SA1 |
| 8 | DM_D10 | DM_D11 | DM_VIO_3 | DM_DQM1 | DM_A5 | Vss40 | AUX_SCL | AUX_SA0 |
| 9 | DM_D12 | DM_D13 | DM_VIO_6 | Vss37 | Vss38 | Vss39 | AUX_SDA | AUX_V33 |
| 10 | DM_D15 | DM_D14 | DM_VIO_5 | DM_CLK1_DH | DM_CLK1_DL | Vss36 | AUX_TDI | AUX_TDO |
| 11 | DM_D1 | DM_D0 | DM_VIO_8 | Vss34 | Vss35 | AUX_V33_1 | AUX_TCK | AUX_TMS |
| 12 | DM_D3 | DM_D2 | DM_VIO_4 | DM_CLK0_DH | DM_CLK0_DL | Vss33 | DNU13 | AUX_PRESENT_N |
| 13 | DM_D5 | DM_D4 | DM_VCC_3 | Vss31 | Vss32 | AUX_V33_0 | AUX_POR_N | AUX_HMR_N |
| 14 | DM_D6 | DM_D7 | DM_VIO_2 | DM_A10 | DM_A2 | Vss30 | AUX_V33_2 | AUX_STANDBY_N |
| 15 | DM_DQS0_DH | DM_DQS0_DL | DM_VIO_7 | DM_WE_N | DM_CS1_N | Vss29 | DNU7 | DNU8 |
| 16 | DM_D16 | DM_D17 | DM_VCC_2 | DM_DQM0 | DM_A13 | NA_VIO_2 | NA_IO15 | NA_IO7 |
| 17 | DM_D19 | DM_D18 | DM_VCC_1 | DM_RAS_N | DM_CAS_N | Vss28 | NA_IO14 | NA_IO6 |
| 18 | DM_D22 | DM_D20 | DM_VIO_1 | DM_BA1 | DM_BA0 | Vss27 | NA_IO13 | NA_IO5 |
| 19 | DM_D23 | DM_D21 | DM_VIO_0 | DM_A1 | DM_A0 | Vss26 | NA_IO12 | NA_IO4 |
| 20 | DM_DQS2_DH | DM_DQS2_DL | DM_VCC_0 | DM_DQM2 | DM_A3 | Vss25 | NA_IO11 | NA_IO3 |
| 21 | Vss20 | Vss21 | Vss22 | Vss23 | Vss24 | NA_VIO_1 | NA_IO10 | NA_IO2 |
| 22 | SM_D23 | SM_D31 | SM_V33_2 | SM_A30 | SM_A31 | Vss19 | NA_IO9 | NA_IO1 |
| 23 | SM_D22 | SM_D30 | SM_V33_1 | SM_A28 | SM_A29 | Vss18 | NA_IO8 | NA_IO0 |
| 24 | SM_D21 | SM_D29 | SM_V33_0 | SM_A26 | SM_A27 | Vss17 | DNU12 | NA_PRE |
| 25 | SM_D20 | SM_D28 | SM_VIO_8 | SM_A24 | SM_A25 | Vss16 | NA_RY | NA_RE_N |
| 26 | SM_D19 | SM_D27 | SM_VIO_7 | SM_A22 | SM_A23 | NA_VIO_0 | NA_CS3_N | NA_VIO |
| 27 | SM_D18 | SM_D26 | SM_VIO_6 | SM_A20 | SM_A21 | NA_V33_0 | NA_CS2_N | NA_CS1_N |
| 28 | SM_D17 | SM_D25 | SM_VIO_5 | SM_A18 | SM_A19 | NA_V18_0 | NA_CLE | NA_ALE |
| 29 | SM_D16 | SM_D24 | SM_CLK3 | SM_A16 | SM_A17 | Vss15 | NA_WE_N | NA_WP_N |
| 30 | DNU16 | Vss12 | SM_CLK2 | Vss13 | SM_BE2 | Vss14 | DNU5 | DNU6 |
| 31 | DNU17 | Vss9 | SM_CLK1 | Vss10 | SM_BE3 | SM_OE_N | Vss11 | DNU4 |
| 32 | SM_D7 | SM_D15 | SM_CLK0 | SM_A14 | SM_A15 | SM_WE_N | Vss8 | DNU3 |
| 33 | SM_D6 | SM_D14 | SM_VIO_4 | SM_A12 | SM_A13 | SM_LBA_N | Vss7 | SM_WP_N |
| 34 | SM_D5 | SM_D13 | SM_VIO_3 | SM_A10 | SM_A11 | SM_BUSY_N | Vss6 | SM_RESET_N |
| 35 | SM_D4 | SM_D12 | SM_VIO_2 | SM_A8 | SM_A9 | SM_BWAIT_N | Vss5 | SM_PD |
| 36 | SM_D3 | SM_D11 | SM_VIO_1 | SM_A6 | SM_A7 | Vss4 | DNU1 | DNU2 |
| 37 | SM_D2 | SM_D10 | SM_VIO_0 | SM_A4 | SM_A5 | Vss3 | SM_IRQ_N | SM_CS3_N |
| 38 | SM_D1 | SM_D9 | SM_V18_2 | SM_A2 | SM_A3 | Vss2 | SM_CRE | SM_CS2_N |
| 39 | SM_D0 | SM_D8 | SM_V18_1 | SM_A0 | SM_A1 | Vss1 | SM_DMARQ_N | SM_CS1_N |
| 40 | DNU14 | DNU15 | SM_V18_0 | SM_BE0 | SM_BE1 | Vss0 | DNU0 | SM_CS0_N |



PISMO2-00021: Micron Mobile DRAM + NAND Module Pin Assignments and Descriptions

Table 6 lists and briefly describes all (and only) the signals that are routed to and from the memory devices installed on the PISMO2-00021, with reference to the corresponding bottom connector ball.

Table 6: PISMO2-00021 Ball Description (Referenced to the Bottom Connector)

| Ball No. (Bottom) | Symbol | Type | Description |
|---|--------------------------|-------|---|
| DRAM Section | | | |
| D12, E12 | DM_CLK0_DH DM_CLK0_DL | Input | System clock: DM_CLK_DH and DM_CLK_DL are differential clock inputs. All address and control input signals are sampled on the positive edge of DM_CLK_DH and the negative edge of DM_CLK_DL. Output (read) data is referenced to both edges of DM_CLK. Internal clock signals are derived from DM_CLK_DH/DM_CLK_DL. SDRAM and Mobile SDRAM only use DM_CLK_DH. Both DM_CLK_DH and DM_CLK_DL apply to DDR, Mobile DDR, and DDR2 SDRAM. |
| E5 | DM_CKE0 | Input | Clock enable: DM_CKE HIGH activates, and DM_CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking DM_CKE LOW provides PRECHARGE, POWER-DOWN, and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row active in any bank). DM_CKE is synchronous for power-down entry and exit, and for self refresh entry. DM_CKE is asynchronous for self refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the DM_CKE receiver. For proper self refresh entry and exit, DM_VREF must be maintained to this input. DM_CKE must be kept HIGH throughout read and write accesses. |
| E15 | DM_CS0_N | Input | Chip select: DM_CS_N enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when DM_CS_N is registered HIGH. DM_CS_N provides external bank selection on multi-bank systems. DM_CS_N is considered part of the command code. |
| D17 | DM_RAS_N | Input | Row address strobe: Latches row addresses on the positive edge of the DM_CLK with DM_RAS_N LOW. Enables row access and precharge. |
| E17 | DM_CAS_N | Input | Column address strobe: Latches column addresses on the positive edge of the DM_CLK with DM_CAS_N LOW. Enables column access. |
| D15 | DM_WE_N | Input | Write enable: Enables WRITE operation and row precharge. Latches data in starting from DM_CAS_N, DM_WE_N active. |
| D16, D8, D20, E6 | DM_DQM0 to DM_DQM3 | Input | Data input/output mask: Makes data output High-Z, ^t SHZ after the clock and masks the output. Blocks data input when DM_DQM active. |
| E18, D18 | DM_BA0, DM_BA1 | Input | Bank select address: DM_BA0 and DM_BA1 define which bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied to. Bank address also determines whether the mode register or extended mode register is to be accessed during an MRS or EMRS cycle. |
| E19, D19, E14, E20, E2, E8, E3, D3, D7, E4, D14, D4, E7 | DM_A0 to DM_A12 | Input | Address: Row/column addresses are multiplexed on the same pins. |



PISMO2-00021: Micron Mobile DRAM + NAND Module Pin Assignments and Descriptions

Table 6: PISMO2-00021 Ball Description (Referenced to the Bottom Connector) (Continued)

| Ball No. (Bottom) | Symbol | Type | Description |
|--|--------------------------|--------|--|
| B11, A11, B12, A12, B13, A13, A14, B14, A7, B7, A8, B8, A9, B9, B10, A10, A16, B16, B17, A17, B18, B19, A18, A19, B2, B3, A2, A3, B4, A4, A5, B5 | DM_D0 to DM_D31 | I/O | Data input/output: Data inputs/outputs are multiplexed on the same pins. |
| A15, A6, A20, A1 | DM_DQS0_DH to DM_DQS3_DH | I/O | Data strobes: Output with read data, input with write data. Edge-aligned with read data, centered in write data. Only applicable to DDR and DDR2 SDRAM. |
| C19, C18, C14, C8, C12, C10, C9, C15, C11, C7 | DM_VIO_0 to DM_VIO_9 | Supply | Data output power: Isolates the output buffer power supply to provide improved noise immunity. |
| C20, C17, C16, C13 | DM_VCC_0 to DM_VCC_3 | Supply | Power supply: Power for the core logic. |
| E16 | DM_A13 | Input | Upgrade address input for future devices (selected via R5). |
| NAND Flash Section | | | |
| H28 | NA_ALE | Input | Address latch enable: Controls the address registers. When active (HIGH), an address is latched from NA_IO0–NA_IO7 into the address registers with the rising edge of the write enable signal. When addresses are not being loaded, NA_ALE is driven LOW. |
| H27, G27 | NA_CS0_N, NA_CS1_N | Input | Chip enable (active-LOW signal): These device select control signals are active (LOW) and are ignored during any of the busy states. The NAND devices go into a low-power standby mode when driven HIGH during ready states. The host should implement as many chip select signals as supported by the host CPU, starting at NA_CS0_N and pulling-up all remaining NA_CSN_N signals to NA_VIO. |
| G28 | NA_CLE | Input | Command latch enable: Controls the command register. When active (HIGH), commands are latched from NA_IO0–NA_IO7 into the register with the rising edge of the write enable signal. When a command is not being loaded, this signal is driven LOW. |
| H25 | NA_RE_N | Input | Read enable (active-LOW signal): Initiates the transfer of information from the device to the host and increments the internal column counter by one. Information is valid when it is active (LOW) and is driven HIGH when information is not being transferred. |
| G29 | NA_WE_N | Input | Write enable (active-LOW signal): Initiates the transfer of information from the host to the device. Command, address, and data are latched with the rising edge and WE is driven HIGH when information is not being transferred. |
| H29 | NA_WP_N | Input | Write protect (active-LOW signal): Provides a hardware method for protecting NAND memory contents. LOW means write-protected. |
| H23, H22, H21, H20, H19, H18, H17, H16, G23, G22, G21, G20, G19, G18, G17, G16 | NA_IO0 to NA_IO15 | I/O | Data inputs and outputs: These bidirectional signals are used to input command and address. They can input data during WRITE operation and output data during READ operation. All signals are inputs during non-READ operations. |



PISMO2-00021: Micron Mobile DRAM + NAND Module Pin Assignments and Descriptions

Table 6: PISMO2-00021 Ball Description (Referenced to the Bottom Connector) (Continued)

| Ball No. (Bottom) | Symbol | Type | Description |
|---|---------------------------|--------|---|
| G25 | NA_RY | Output | Ready/Busy: Indicates the operating condition of the device. It is busy, active (LOW) during PROGRAM, ERASE, and READ operation and returns to ready, active (HIGH) after completing the operation. This signal is an open drain output buffer on memory modules. The host must implement a pull-up resistor to NA_VIO. The value of this pull-up resistor determines the rise time of the NA_RY signal and should be calculated as specified in the NAND Flash memory data sheets. |
| F28 | NA_V18_0 | Supply | 1.8V power supply: The host implementation supplies 1.8V DC on this pin, independent of the I/O voltage. This power supply is used as memory core voltage. |
| EEPROM Section | | | |
| H9, H8, H7 | AUX_SA0 to AUX_SA2 | Input | Used by the EEPROM for multiple device operation. The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the comparison is true. Up to eight devices may be connected to the same bus by using different chip select bit combinations. |
| G8 | AUX_SCL | Input | Synchronizes data transfer to and from the device. |
| G9 | AUX_SDA | I/O | This bidirectional pin transfers addresses and data into and data out of the device. It is an open drain terminal; therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10kΩ for 100 kHz, 2kΩ for 400 kHz). For normal data transfer, SDA is allowed to change only during SCL LOW. Changes during SCL HIGH are reserved for indicating start and stop conditions. |
| F13, F11, G14 | AUX_V33_0 to AUX_V33_2 | Supply | 1.8V to 5.5V power supply. |
| Ground Pins | | | |
| F40, F39, F38, F37, F36, G35, G34, G33, G32, B31, D31, G31, B30, D30, F30, F29, F25, F24, F23, F22, A21, B21, C21, D21, E21, F20, F19, F18, F17, F15, F14, D13, E13, F12, D11, E11, F10, D9, E9, F9, F8, F7, F6, F5, F4, F2, E1 | Vss0 to Vss46 | Supply | Ground. |

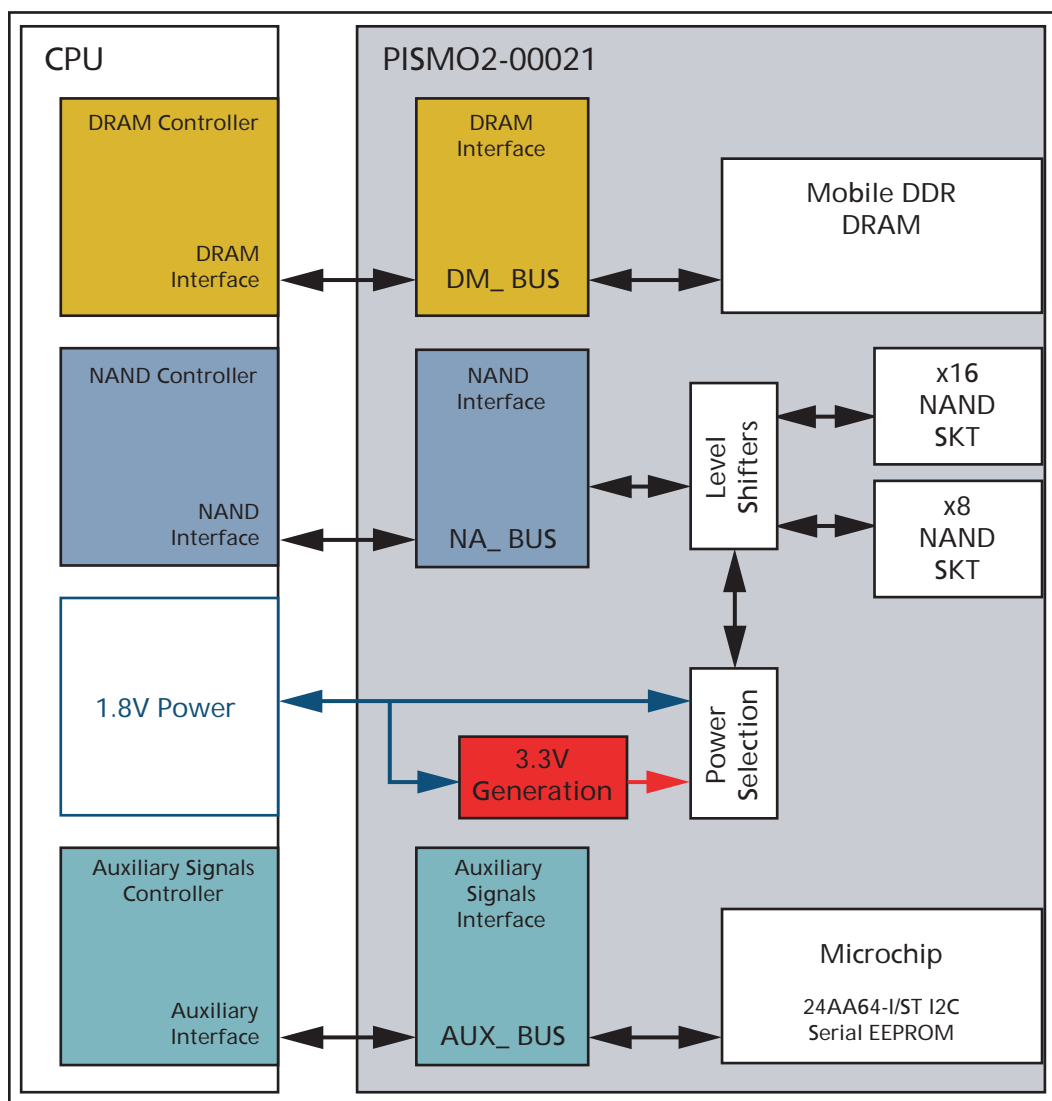


Functional Block Diagram

Figure 2 illustrates the connections between the host system, the PISMO2-00021 DRAM and NAND interface, the Micron DRAM, and the NAND sockets. All NAND and DRAM interface signals are also connected straight through from bottom to top on the PISMO2 connector, except NA_CS[3:0] and DM_CS[1:0], which are shifted by one. See “Chip Select Routing” on page 10 for more information. The STATIC and FAST SERIAL interface signals are only “routed through” (no devices are connected).

In Figure 2, the NAND and DRAM interface signal connections have been omitted for clarity.

Figure 2: PISMO2-00021 Functional Block Diagram





Chip Select Routing

The PISMO2 specification enables the DRAM interface to support up to two memory banks, adopting the same signaling, whereas up to four memory banks can be connected to the STATIC interface and four to the NAND interface. The PISMO2-00021 memory module uses one DRAM and one NAND bank. Table 7 clarifies the chip select routing scheme adopted for this implementation. This method automatically maps host controller chip select signals to the NAND memory banks installed within a PISMO2 memory module stack.

If the number of stacked memory banks exceeds host controller support, only the first two DRAM, the first four static, and the first four NAND banks (starting at the bottom-most module) are used. All remaining banks are forced inactive.

Table 7: PISMO2-00021 DRAM and NAND Interface Chip Select Routing

| Memory Interface | Chip Select Connections | | Chip Select Routing |
|--|--|--|---------------------|
| | Bottom Side | Top Side | |
| DRAM interface: - 1 device installed - 1 CS_N used | DM_CS0_N DM_CS1_N DM_VIO | To Mobile DDR DM_CS0_N DM_CS1_N | |
| NAND interface: - 1 device installed - 2CS_N used | NA_CS0_N NA_CS1_N NA_CS2_N NA_CS3_N NA_VIO | To NAND SKT To NAND SKT NA_CS0_N NA_CS1_N NA_CS2_N NA_CS3_N | |

Design for Testability

Although the PISMO2 specification prohibits routing used chip selects back to the top connector, the PISMO2-00021 board features a configuration option that allows the user to scope CS# with the Micron PISMO2-P6960 logic state analyzer tile. Every chip select signal that is connected to an installed memory chip can be routed back to the higher CS# position available for the bank on the top connector, just by moving a configuration resistor. (For example, the NA_CS0_N ball of the bottom connector is also connected to NA_CS2_N position of the top connector by R29.) Configuration options are listed in Table 8 on page 11. See the PISMO2-P6960 data sheet for more information.


Table 8: PISMO2-00021 CS# Feedback Configurations

| Configuration Resistor | Signal | Top Connector Position | Notes |
|------------------------|----------|------------------------|--|
| R12 | DM_VIO | D1 | If R12 is installed, the board is compliant with the PISMO2 specification |
| R13 | DM_CS0_N | D1 | If R13 is installed, the CS is routed back to the top connector |
| R205 | NA_POWER | H26 | If R205 is installed, the board is compliant with the PISMO2 specification |
| R9 | NA_CS0_N | H26 | If R9 is installed, the CS is routed back to the top connector |
| R206 | NA_POWER | G26 | If R206 is installed, the board is compliant with the PISMO2 specification |
| R15 | NA_CS1_N | G26 | If R15 is installed, the CS is routed back to the top connector |

Serial Presence Detect

The Micron PISMO2-00021 module features serial presence-detect (SPD). The SPD function is implemented using a 64Kb serial EEPROM compliant with the PISMO2 specification. This nonvolatile storage device contains 8KB. System READ/WRITE operations between the master (host system) and the slave EEPROM device occur via a standard I²C bus using the PISMO2-00021 AUX_SCL (clock) and AUX_SDA (data) signals, together with AUX_SA[2:0], which provide eight unique PISMO2/EEPROM addresses. The memory write protect pin (WP#) is tied to ground on the module, permanently disabling hardware write protect. All these signals are in the AUX_V33 I/O voltage domain, which is fixed at 3.3V.

The configuration EEPROM contains information about the memory module itself, such as vendor, complete part number, and serial number. It also contains information about the memory devices installed on the module. The operating system or the application running on the host system processor can use the data from the configuration EEPROM to perform the following tasks:

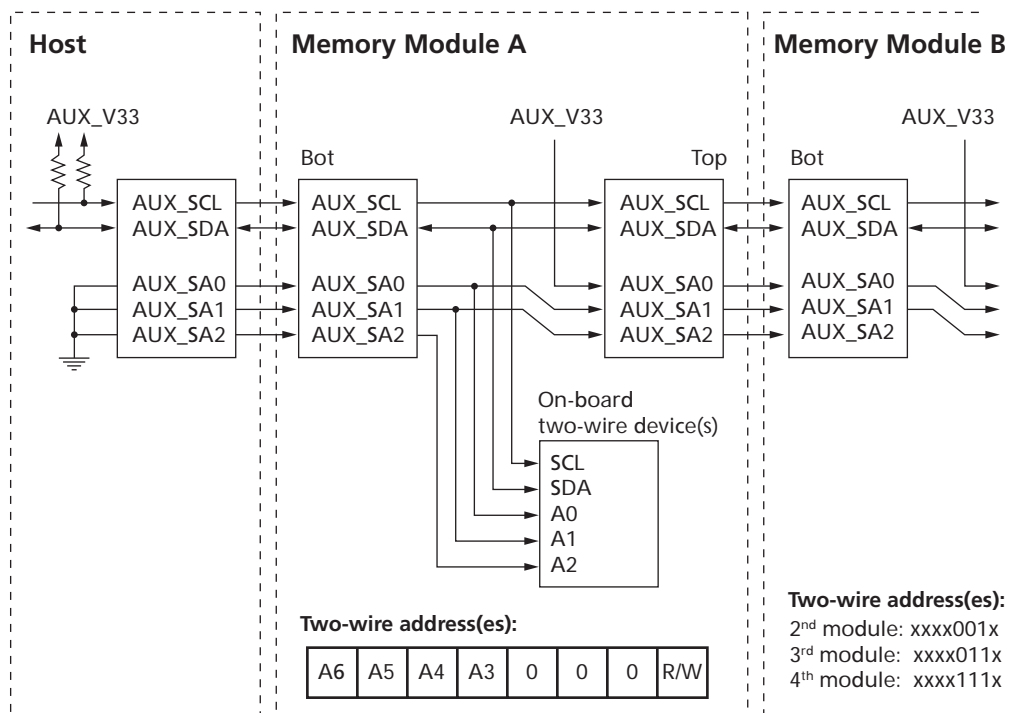
- Initialize the memory space
- Identify the PISMO2 memory card vendors, model, and revision
- Validate system configurations
- Query product names of installed memory devices in terms of speed grade, data bus width, density of memory chip, and addressing scheme
- Query key memory device parameters, such as timing and voltage options
- Optimize host controller settings according to detected memory parameters
- Select optimized programming algorithms
- Select software drivers based on identified memory modules
- Obtain additional vendor-specific information

The Micron PISMO2-00021 board complies with the PISMO 2.0 specification, which defines a scheme for automatically assigning two-wire addresses to two-wire devices on the memory module. As shown in Figure 3, the PISMO2-00021 module automatically assigns two-wire device addresses by module location in the stack. No additional logic is required for this function.



PISMO2-00021: Micron Mobile DRAM + NAND Module Serial EEPROM Data Structure

Figure 3: PISMO2-00021 Two-Wire Address Generation Scheme



The connections shown in Figure 3 result in the two-wire device address assignments shown in Table 9.

Table 9: EEPROM Addresses

| Memory Module Stack Location | EEPROM Address (Hexadecimal) |
|--|------------------------------|
| 1 st memory module (bottommost) | 0xA0 (WRITE), 0xA1 (READ) |
| 2 nd memory module | 0xA2 (WRITE), 0xA3 (READ) |
| 3 rd memory module | 0xA6 (WRITE), 0xA7 (READ) |
| 4 th memory module (topmost) | 0xAE (WRITE), 0xAF (READ) |

Serial EEPROM Data Structure

TBD



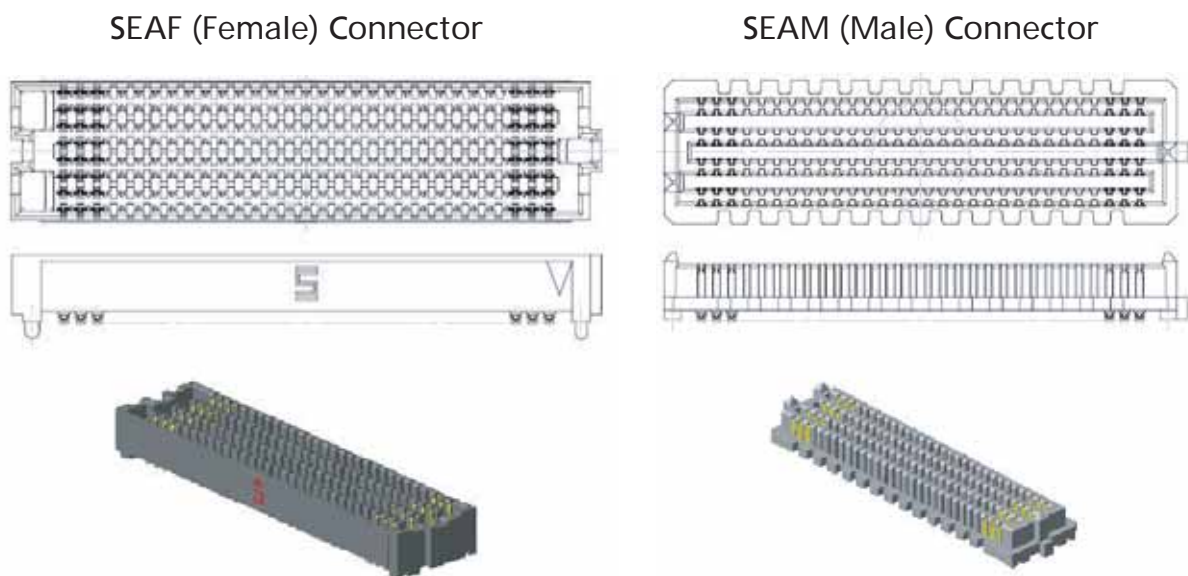
Mechanical Specifications

Connector Description

The PISMO2-00021 board/host system connection is provided by a Samtec SE (single-ended) array connector system designed for high-speed/high-density applications where high pin-count flexibility, space savings, and routability are critical. The Edge Rate™ blade and beam interface was designed to provide maximum signal integrity at 50Ω on a popular 0.050in x 0.050in grid. The SE array connector has been tested up to 4 GHz (single ended) and 9 GHz (differentially) at the 7mm mated height.

Figure 4: PISMO2 Connectors

For clarity, some contacts are not shown



Connector Specifications

- Male P/N: SEAM-40-02.0-SM-8-2-A-K
- Female P/N: SEAF-40-05.0-SM-8-2-A-K
- Black liquid crystal polymer
- 320 positions (8 x 40 grid)
- 1.27mm (0.050in) pitch
- 7mm mated height
- 30 microinch Au duplex contact plating
- Copper alloy contact material
- -55°C to +125°C operating temperature range
- Pb-free solder

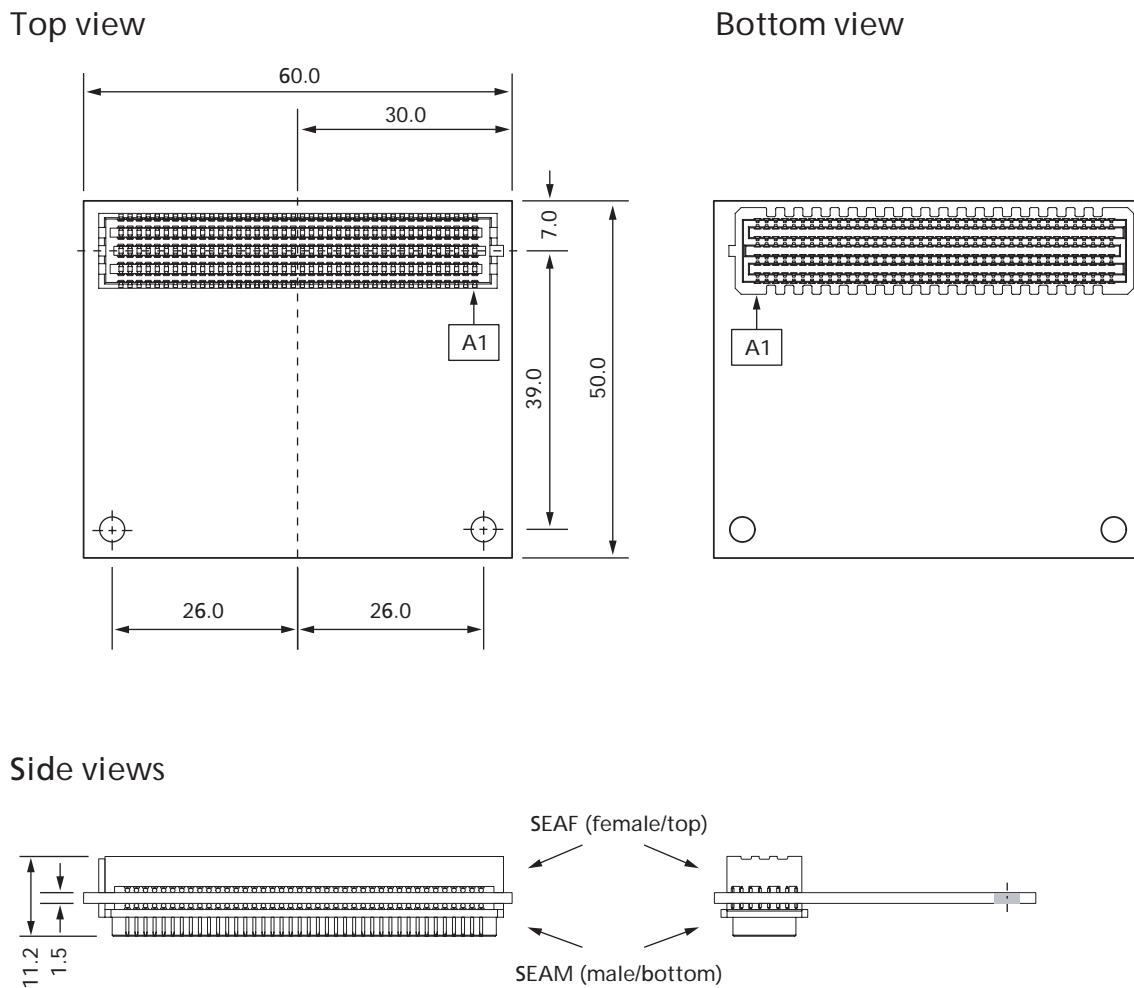


PISMO2-00021: Micron Mobile DRAM + NAND Module Mechanical Specifications

Memory Module

Figure 5 illustrates the mechanical construction of the PISMO2-00021 memory module. The A1 mark denotes the location of the A1 pin on both connectors.

Figure 5: PISMO2-00021 Memory Module Dimensions



The bottom side is used as the primary assembly side. The top side carries module documentation, such as the label.



Vertical Space

The connectors chosen for PISMO2 use a 7mm stacked height. This means that a 7mm vertical space exists between the host system and the first memory module PCBs and also between the PCBs of the two neighboring memory modules. The PISMO2 specification defines requirements for vertical space assignments on PISMO2 memory modules and host controllers. Because Micron's PISMO2-00021 complies with this requirement, it can be plugged into any PISMO2 host controller or on top of any other memory module. Figure 6 illustrates the PISMO2 vertical space requirements.

Figure 6: PISMO2-00021 Vertical Space Requirements

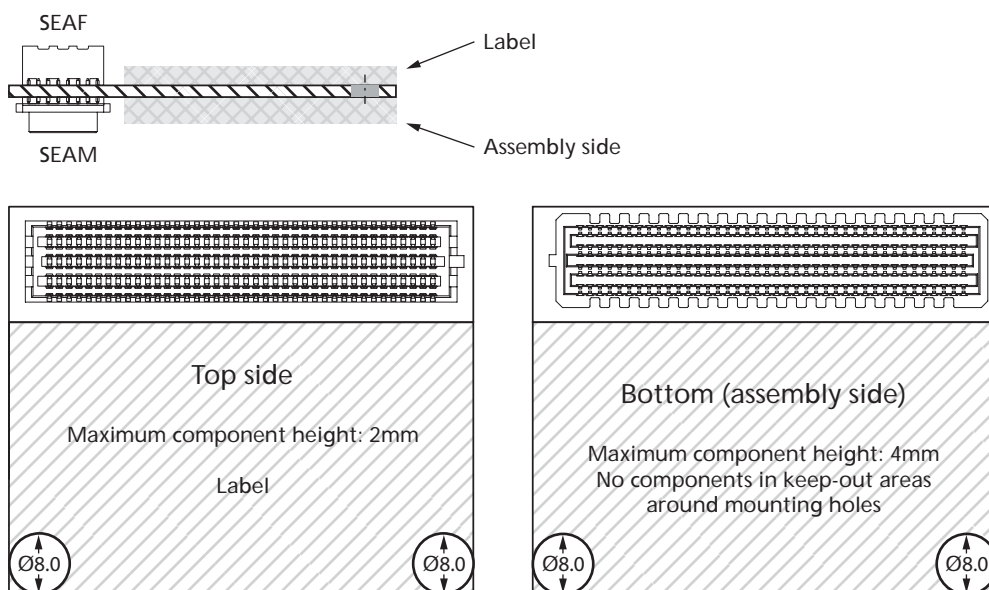
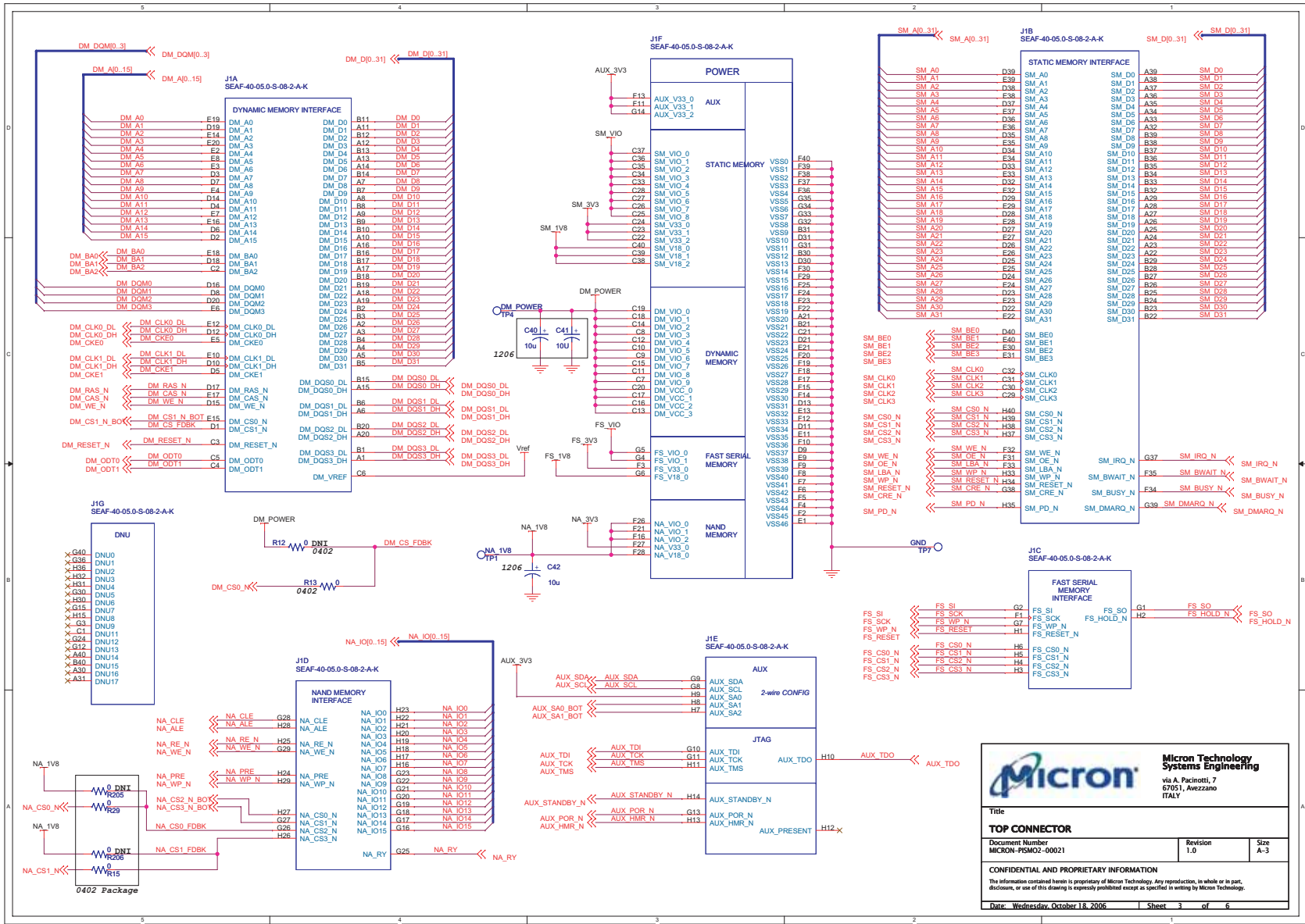


Figure 8: Top Connector Schematic



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 67051, Avezzano
 ITALY

TOP CONNECTOR

Document Number: MICRON-PISMO2-00021

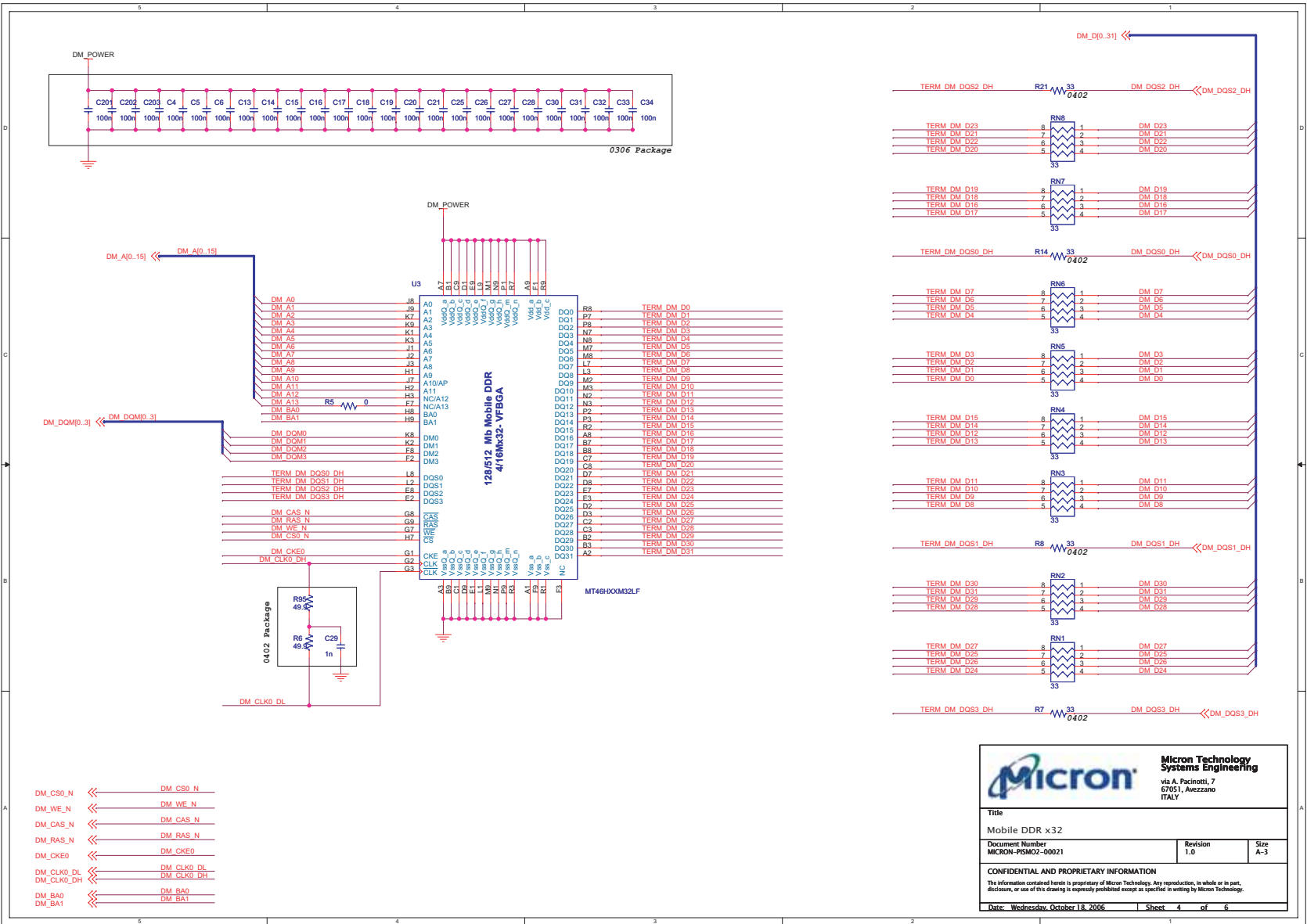
| | |
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| Revision 1.0 | Size A-3 |
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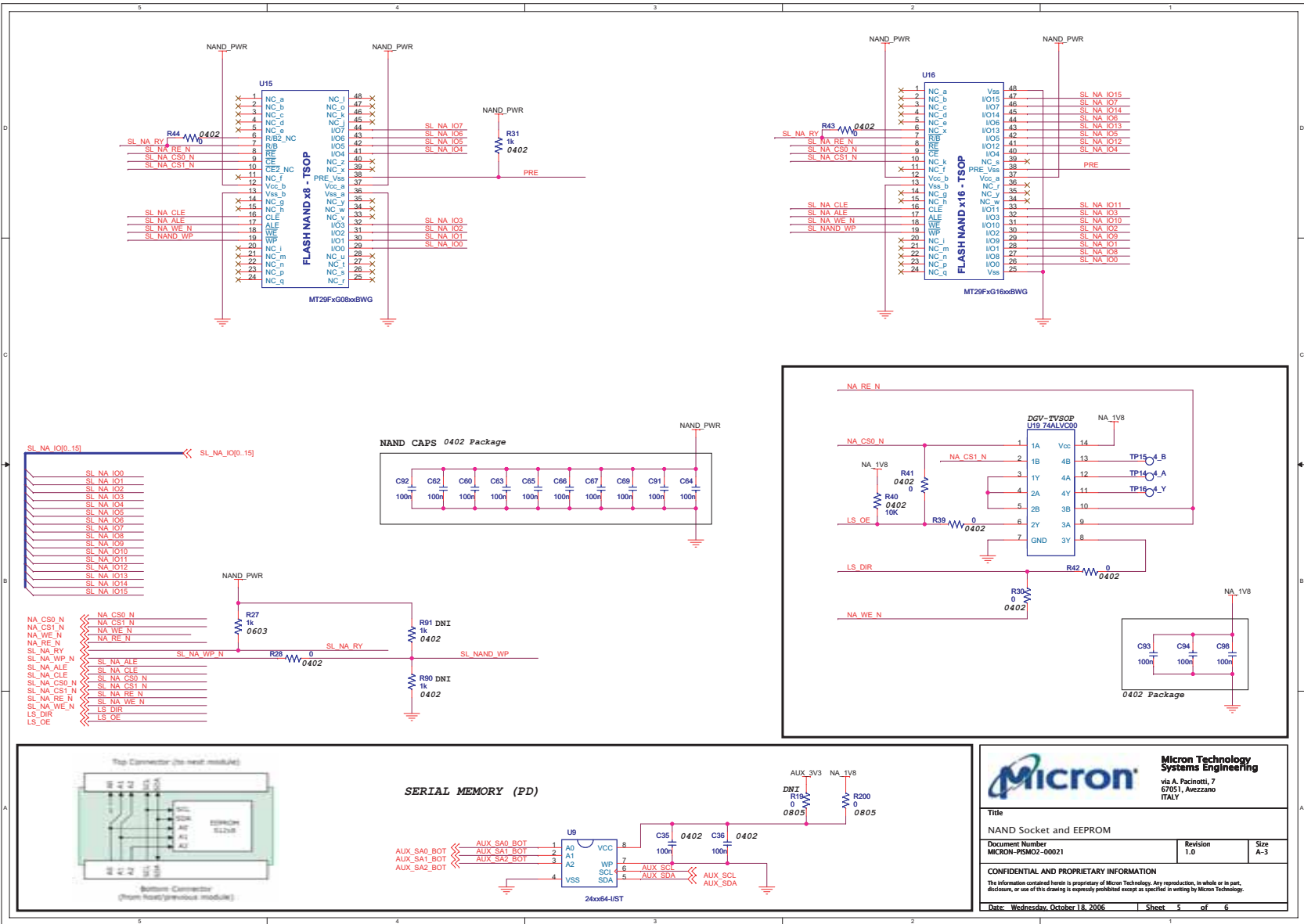
Date: Wednesday, October 18, 2006 Sheet 3 of 6

Figure 9: Mobile DDR SDRAM Interface Schematic



| | | |
|--|-------------------------|---------------------|
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| <p>Title Mobile DDR x32</p> | | |
| <p>Document Number MICRON-PISMO2-00021</p> | <p>Revision 1.0</p> | <p>Size A-3</p> |
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Figure 10: NAND Flash and EEPROM Interface Schematic



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Title
 NAND Socket and EEPROM

Document Number
 MICRON-PISMO2-00021

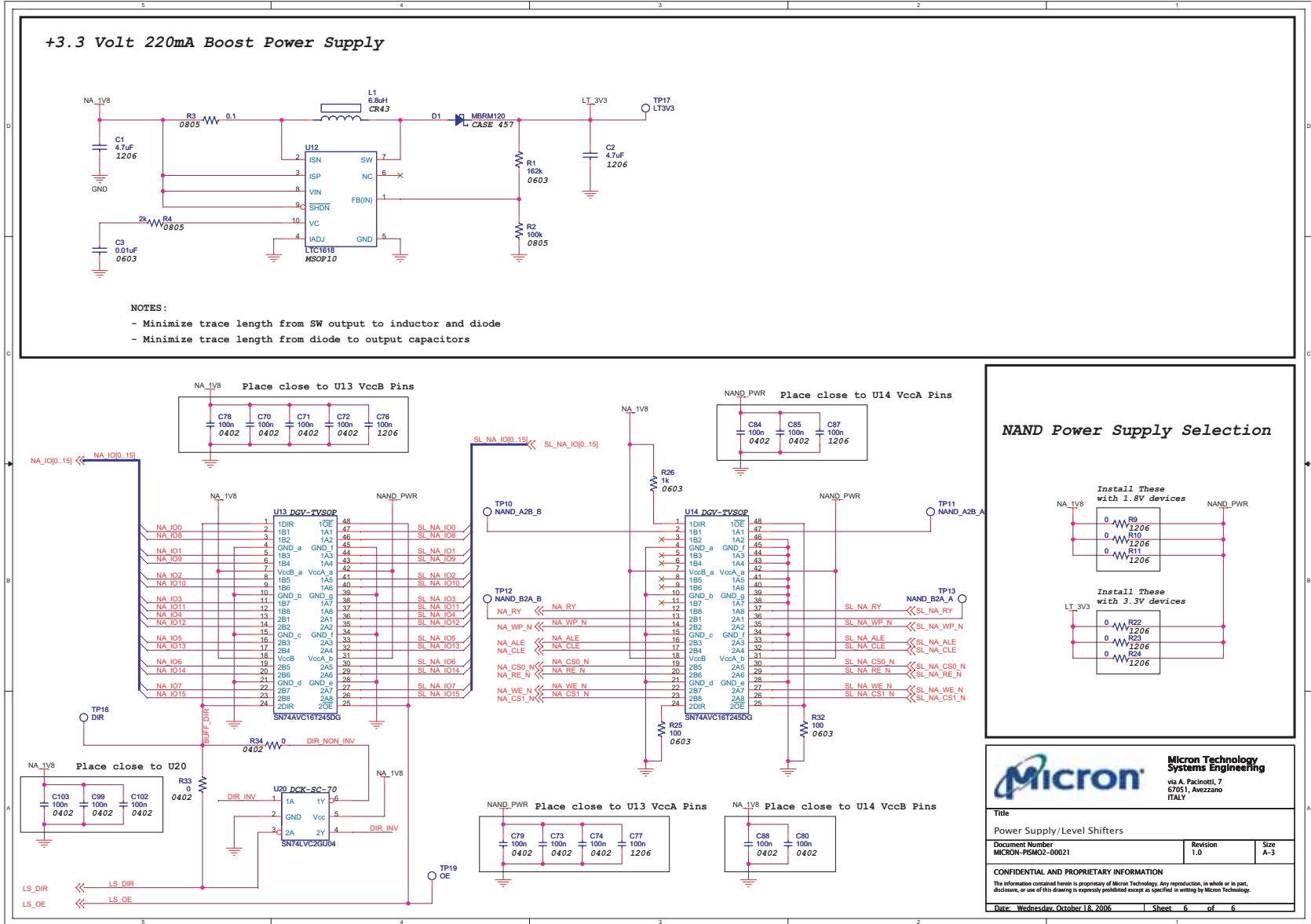
Revision
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Size
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Figure 11: Power Supply/Level Shifters Schematic





PISMO2-00021: Micron Mobile DRAM + NAND Module Appendix A: Part Numbering and Reference Documents

Appendix A: Part Numbering and Reference Documents

Figure 12: PISMO2-00021 Part Number Diagram

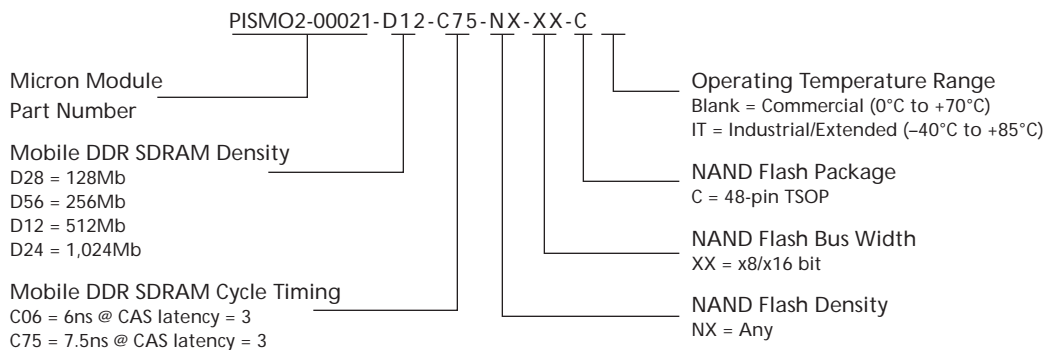


Table 10: Reference Documents

| Document Description | Manufacturer | Part Numbers | Revision Date |
|---|-------------------|---------------------------------|---------------------|
| PISMO2 specification | - | - | V. 1.01, 05/03/2006 |
| 1Gb NAND Flash data sheet | Micron | MT29F1G8AB MT29F1G16AB | Rev. A, 5/05 |
| 2Gb NAND Flash data sheet | Micron | MT29F1G8ABA MT29F2G16ABA | Rev. A, 5/05 |
| 128Mb Mobile DDR SDRAM data sheet | Micron | MT46H4M32LF | Rev. 1.0, 08/05 |
| 256Mb Mobile DDR SDRAM data sheet | Micron | MT46H8M32LF | Rev. B, 1/05 |
| 512Mb Mobile DDR SDRAM data sheet | Micron | MT46H16M32LF | Rev. G, 11/05 |
| 1Gb Mobile DDR SDRAM data sheet | Micron | MT46H32M32LF | TBD |
| 16-bit transceiver data sheet | Texas Instruments | SN74AVC16T245DGGR (SCES551C) | August 2005 |
| 1.4 MHz step-up DC/DC converter data sheet | Linear Technology | LT 1618 | - |
| Quadruple 2-input positive-NAND gate data sheet | Texas Instruments | SN74ALVC00 (SCES115G) | August 2004 |
| Dual inverter gate data sheet | Texas Instruments | SN74LVC2GU04 (SCES197K) | July 2005 |
| PISMO2-P6960 LSA adapter tile data sheet | Micron | PISMO2-P6960 | Rev. A, 1/07 |
| Serial EEPROM data sheet | Microchip | 24AA64-I/ST I2C | 11/15/2002 |

Notes: 1. Micron data sheets can be downloaded from www.micron.com.



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