



RLDRAM® II Memory

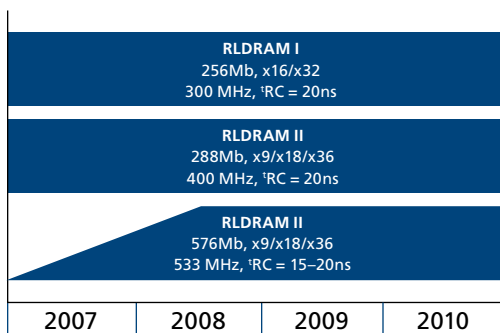
Low-Latency, High-Density, High-Bandwidth DRAM

The second generation of reduced-latency DRAM (RLDRAM®) is a high-performance memory that combines the performance-critical features that networking, image processing, and cache applications need, such as high density, high bandwidth, and fast SRAM-like random access.

The key to the RLDRAM II performance is its innovative circuit design, which minimizes the time between the beginning of the access cycle and the availability of the first data. Plus, RLDRAM II memory offers bank cycle times of 15ns to 20ns, which is three times shorter than DDR SDRAM.

RLDRAM II technology provides minimized latency and reduced row cycle times that are ideal for applications, such as networking, image processing, and cache, which require critical response times and very fast random access. Its impressive feature set provides the optimal cost/performance and density parameters that give RLDRAM II memory the flexibility to perform in a wide range of applications.

RLDRAM Product Road Map



RLDRAM Ecosystem

RLDRAM II is supported by many controllers targeted for general purpose memory interface or specific system applications. RLDRAM ecosystem controllers include:*

- | | |
|------------------|-----------------------|
| Agere | Lattice Semiconductor |
| Altera | LSI Logic |
| AMCC | Marvell |
| Broadcom | MathStar |
| Bay Microsystems | Raza Microelectronics |
| Cavium | Sensory Networks |
| CSwitch | T-Pack |
| Dune Networks | Xelerated |
| EZ Chip | Xilinx |

*Micron does not imply these companies are partners in RLDRAM developments.

288Mb Specifications

- 288Mb organized as 8 Meg x 36, 16 Meg x 18, and 32 Meg x 9
- 400 MHz double data rate operation (800 Mb/s/pin)
- Sustained data bandwidth of 3.6 GB/s with random bank accesses (x36 device)
- Low row cycle time of 20ns

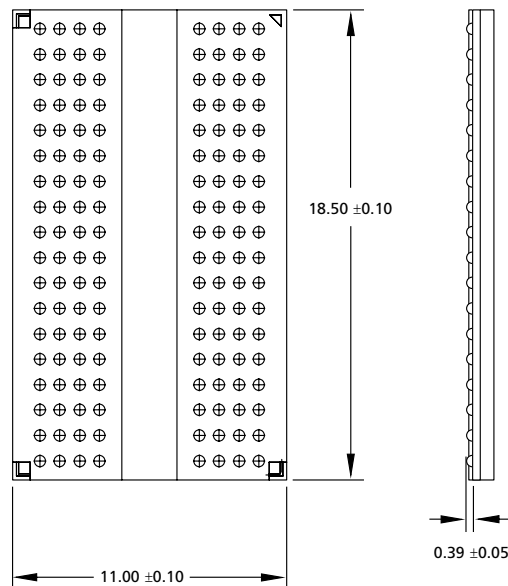
576Mb Specifications

- 576Mb organized as 16 Meg x 36, 32 Meg x 18, and 64 Meg x 9
- 533 MHz double data rate operation (1,066 Mb/s/pin)
- Sustained data bandwidth of 4.8 GB/s with random bank accesses (x36 device)
- Low row cycle time of 15–20ns

RLDRAM II Features

- Eight internal memory banks
- Multiplexed and nonmultiplexed address modes
- Differential input clocks
- Differential read and write clocks
- On-chip DLL for accurate output data placement
- Data valid signal for simplified data capture
- Programmable burst lengths of 2, 4, and 8
- Data mask signal for masking write data during bursts
- 1.8V core/2.5V external and 1.5V or 1.8V I/O
- Variable calibrated matched impedance I/O
- Intelligent on-die termination (ODT)
- Common and separate I/O configurations
- IEEE 1149.1-compatible JTAG boundary scan

To find out how RLDRAM II memory can improve your application's performance, call Micron product marketing at 208-368-3900. For technical documents and support, see www.micron.com/rldram.



144-Ball FBGA Package

The footprint of the RLDRAM II 144-ball FBGA package is 22 percent smaller than that of a standard 66-pin TSOP.

www.micron.com

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