Osmium™ Packaging Technology

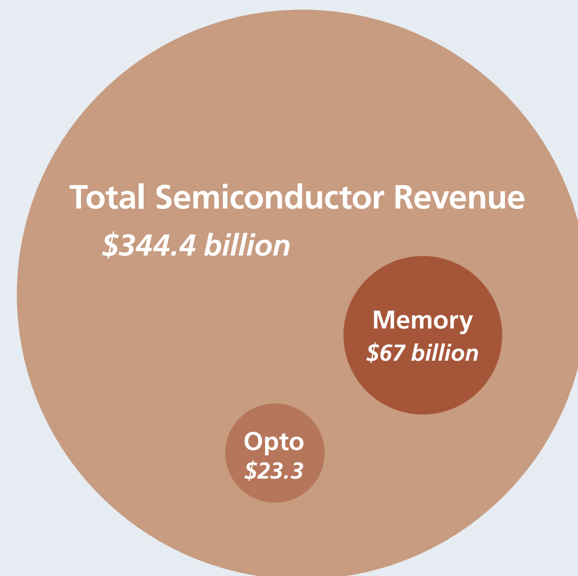
The Integrated Circuit – Electronics' First Golden Age

The invention of the integrated circuit in 1958 marked one of the most significant advances of our time. The advent of transistors in 1947 had been a stunning achievement, to be sure, but it left electrical engineers limited, both by the size of the circuits and by the number of components that could be hand-soldered to a circuit board. They knew that if transistors, wires, and other circuit components could be combined in a single form, circuits could be made much smaller, in just one step, and the process could be automated.

The stage was set. Scientists, researchers, engineers, technicians, executives, and marketers were engaged in an exciting exchange of experimental, innovative, inventive ideas. The entire technology industry was caught up in the pursuit of a significant technological advancement when Jack Kilby of Texas Instruments and Robert Noyce of California's Fairchild Semiconductor independently developed the same revolutionary new way of creating electronic circuits. Their pioneering efforts to develop a monolithic, silicon-based, mass-produced integrated circuit marked the beginning of the golden age of modern electronics.

Today, the integrated circuit (IC) that Noyce and Kilby invented can be found everywhere—in every personal computer, mobile phone, video game console; in cars, televisions, and CD players; in virtually all of the electronic devices that the world depends on so completely. The IC has also revolutionized the global economy. Gartner Dataquest (Feb. 2006), for example, estimated that worldwide semiconductor revenue will reach more than $340 billion by 2010. Gartner further projected that approximately $67 billion of that revenue would come from memory products alone and that revenue for optoelectronic semiconductors would reach an estimated $23.3 billion, as illustrated below.

A groundbreaking invention that revolutionizes an entire industry, like the IC did, inevitably relies on the work of many. It's the kind of development that borrows from earlier advancements and blends innovative ideas and unique perspectives.



Projected Semiconductor Revenue by 2010

Reinventing the Packaging Process

A similarly significant technological milestone is on the horizon. This new technology combines three key patented and advanced wafer-level packaging technologies, hundreds of US patents, and years of research and intense analysis. Micron's Osmium™ packaging technology, which borrows its name from one of the densest natural elements known to mankind, promises a plethora of revolutionary uses, reminiscent of the first ICs created nearly 50 years ago.

One reason the development of this technology is so important is because advances in packaging technology have fallen behind the progressive innovations of semiconductor technology. The evolution of the IC package—from ceramic flat packs to dual in-line packages (DIPs), to pin grid array (PGA) and leadless chip carrier (LCC) packages, to ball grid arrays (BGAs), and finally, surface mount packaging and chip-scale packaging—has left much room for improvement. Now, with conventional methods reaching their limits in size, cost, and performance, Osmium technology is poised to drive semiconductor packaging to the wafer level.

Osmium Technology

Micron's Osmium packaging technology encompasses innovations that include through-wafer interconnects, redistribution layer technology, and wafer-level encapsulation, plus hundreds of supporting semiconductor process engineering breakthroughs. Although still in development, this new technique for packaging semiconductor solutions has the potential to deliver memory and imaging devices in ultra-small form factors, eliminate wire bonding, provide extremely high-density memory solutions, and enable an image sensor solution to be packaged in die form.

While specific information about Osmium technology is obviously proprietary and patent protected, an overview of the key technologies and the advantages of extending the fabrication process to finished goods will illustrate the type of increased performance, ease of integration, and size and cost savings that are possible with this new packaging technology.

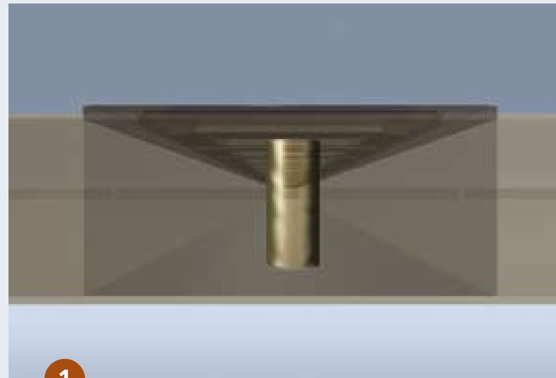
Through-Wafer Interconnects (TWIs)

Until now, semiconductor manufacturing has been focused on a planar or two-dimensional process, building structure upon structure on one side of a silicon wafer. To overcome the obvious limitations of this flat process, most manufacturers (including Micron) have begun stacking die—wire bonding them together to create a denser package.

Die stacking is not without its challenges, however. Because the wire bonds extend beyond the perimeter of the die, the overall size of the package must increase, creating wider x and y values, and in some cases, even higher z (height) values. But size isn't the only issue. The wire bonds limit the electrical performance of high-speed, leading-edge ICs.

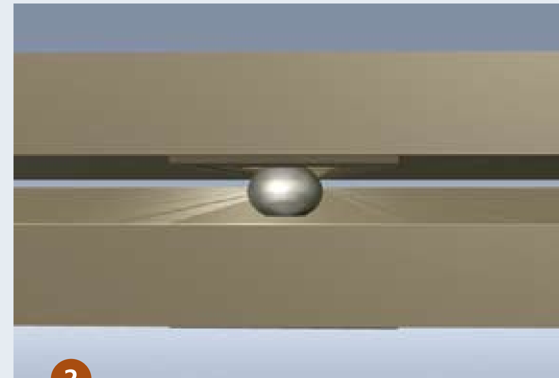
TWI packaging technology overcomes the challenges of package size and device performance. Using advanced fabrication processes, Micron engineers have been able to drill holes directly through a die bond pad and fill the holes with conductive material, creating the shortest possible connection to the bond pad of a second die—enabling die to be stacked on top of one another without wire bonding.

The biggest benefits TWI packaging provides are design-focused and customer-driven: cost, size, and performance. TWIs reduce system costs, create ultra-small form factors, and offer higher potential performance for stacked die.



1

Conductive material fills the small hole directly through the die bond pad



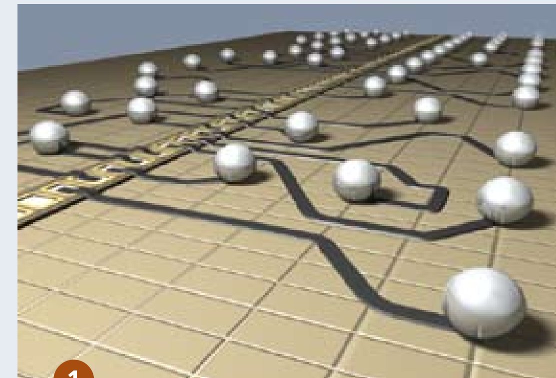
2

Die are stacked using through-wafer interconnections rather than wire bonds on the edge of each die

Redistribution Layer (RDL)

Micron's patented RDL technology enables engineers to have fine control of an IC's timing, while meeting standard and custom ballout patterns for both stacked and monolithic ICs.

RDL also simplifies the bonding process, making it easier and more cost effective to stack die while effectively reducing the z-axis of most packaged parts. In short, the new RDL will give Micron customers higher-density memory products and extraordinary chip-level imaging options.



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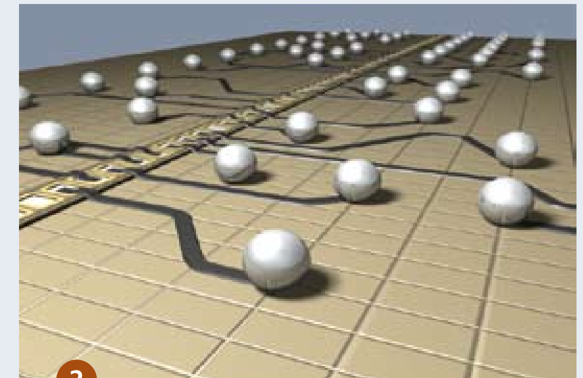
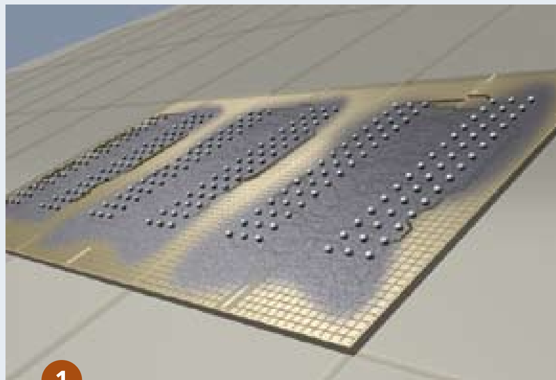


2

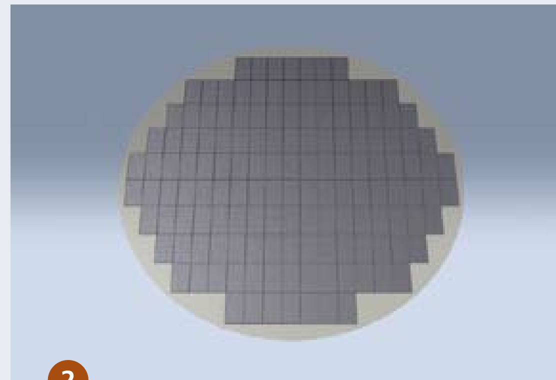
Pad ballouts can be redistributed from the die bond pad to meet standard or custom ballout patterns

Wafer-Level Encapsulation

The third element of Micron's Osmium wafer-level packaging technology is referred to as wafer-level encapsulation. Wafer-level encapsulation uses many advanced semiconductor techniques to completely enclose a die, on all six sides, while it's still part of the wafer. The added value for customers are ease of use, because they're able to work with packaged parts that are mere microns larger than a bare die device, and cost savings, because batch processing die can dramatically increase manufacturing efficiency.



1 *Each die is encapsulated in epoxy on all sides while still part of the wafer*



2 *Die is encapsulated and diced in a batch process in the fab*

Extending the Fab to Finished Goods

Osmium technology is expected to effectively extend Micron's technologically advanced fabs all the way to finished goods—an unparalleled, critical advancement in semiconductor packaging.

Under constant pressure from electronics manufacturers to provide improved performance, smaller packages, and lower costs, semiconductor manufacturers are quickly reaching the limits of what can be achieved with conventional packaging. Today, most techniques involve placing packages on individual die, one by one—a time-consuming and expensive process. And the smaller the die size gets, the more expensive the package becomes.

By using the fab infrastructure for materials, dimensions, and handling, Osmium technology reverses this trend and opens the door for faster and less expensive miniaturization. Osmium technology and the extended fab model are batch processes, working with whole wafers rather than singulated die. At the wafer level, Osmium technology yields the smallest possible package, potentially eliminating lead frames and substrates and enabling hundreds of new technologies. Micron memory devices and CMOS image sensors processed with Osmium wafer-level technology could potentially be manufactured and shipped in packages that are 50 percent smaller than their modern counterparts.

The flipside of creating an ultra-small package using a batch process is a vast reduction in production costs—and comes at a time when current packaging makes up 15 to 25 percent (or more) of the finished product cost. With Osmium technology, the smaller the semiconductor die, or the larger the silicon wafer, the lower the total packaged die cost.

Looking Ahead

Micron's new Osmium technology is the product of a rich patent portfolio, leading-edge technology, market-driven expertise—and a dedicated customer focus. With its unique blend of TWIs, redistribution layer, and encapsulated die in wafer form, Osmium is the right technology at the right time. It's the key to reinventing a process that is quickly reaching its technological limits. And Micron is unlocking the possibilities.

As a digital innovator, Micron is focused on providing advanced technology; IP leadership; and leading design, manufacturing, and supply processes to enhance the competitiveness of our customers' products. Osmium is a perfect example of that. By elevating Osmium technology from an innovative idea to a groundbreaking technological achievement, we intend to change the dynamics of semiconductor manufacturing—and, in the process, set a new standard for smaller, faster, more cost-effective semiconductor solutions. This is how Micron and Osmium technology are fueling digital innovation—by enabling next-generation products that can benefit from the power of this new packaging technology.

About Micron

Micron Technology is one of the world's leading providers of advanced semiconductor solutions. Through its worldwide operations, Micron manufactures and markets DRAM, NAND Flash memory, CMOS image sensors, and other semiconductor components and memory modules for use in leading-edge computing, consumer, networking, and mobile products. For data sheets, technical notes, and other product and sales information, visit our Web site at: *www.micron.com*.

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