

Flash Standards for Embedded Systems

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Abstract

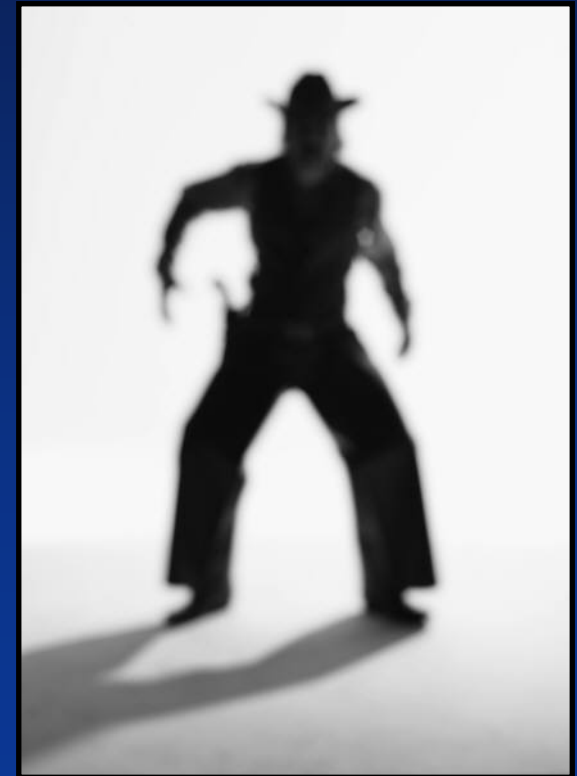
- OEMs are demanding that Flash-based interfaces migrate from a lawless "wild, wild West" frontier to one of defined standards to support interoperability among vendors and to simplify product design, test, and validation
- Take a look at the standards behind controller-less NAND Flash interfaces like the traditional, asynchronous NAND interface and the high-speed, synchronous NAND interface, as well as the standards for controller-based interfaces like BA NAND, e-MMC™, and UFS

Agenda

- No standards: the “wild, wild, West”
- Flash-based interface standards
- The interface “round-up”

No Standards: The “Wild, Wild West”

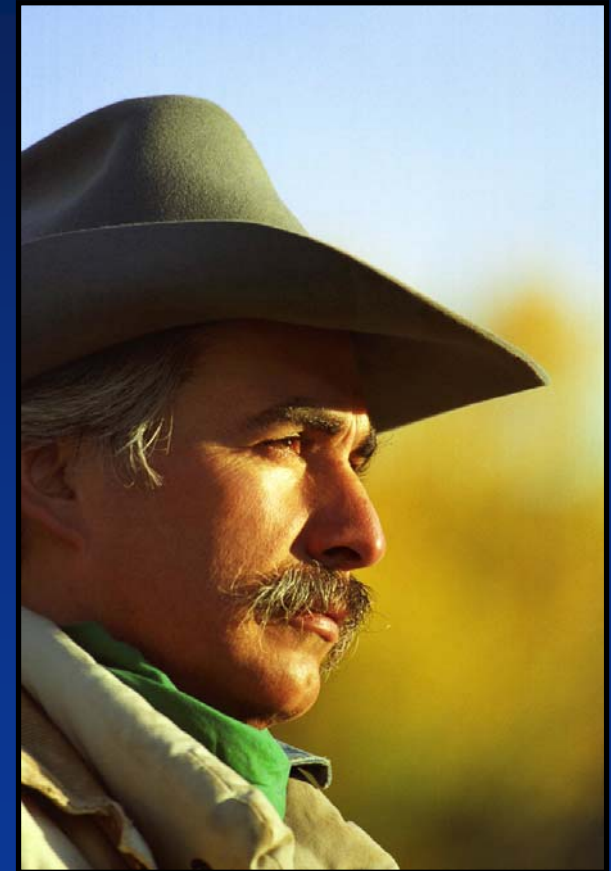
- Standards are needed for device interoperability
- No standards lead to incompatibilities—the “wild, wild West,” which was characterized by:
 - Gunfights and shootouts
 - Lawlessness
 - Robbers



A “Wild, Wild West” Example: NAND Flash

- The NAND Flash interface is a great example of how an interface with no standard became fragmented
 - Lack of consistent device and feature identification
 - Incompatible array architectures and addressing schemes
 - Different command sets
 - Inconsistent device behavior and status

- Result
 - Firmware bandages
 - Long product development/qual cycles
 - Lost revenue from longer time to market
 - The single source trap



Agenda

- No standards: the “wild, wild, West”
- Flash-based interface standards
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Flash-Based Embedded Interface Standards

Standards Organization	Embedded Interface
MMCA/JEDEC	e-MMC
JEDEC	UFS
ONFI	NAND
	Source-synchronous NAND
	BA NAND
SDA	eSD

Two Types of Interfaces

▪ Raw

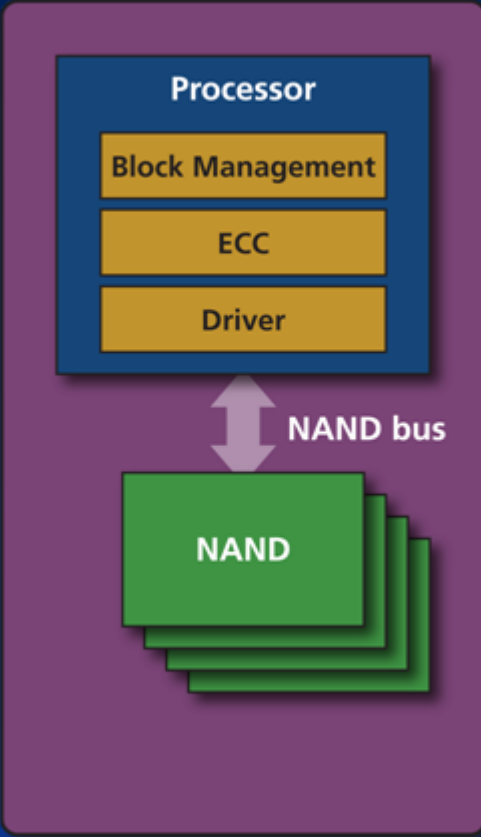
- The NAND memory is directly controlled by the host processor/controller
- The host processor provides ECC, wear-leveling, and block management
- The host processor deals with NAND architecture differences including page size, block size, # of planes, array performance
- Lower cost per bit

▪ Managed

- The NAND memory is buffered by an interface controller in the same package as the NAND
- The interface controller provides ECC, wear-leveling, and block management
- The interface controller hides the NAND architecture and provides fixed data sector sizes to the host
- Lower up-front development cost

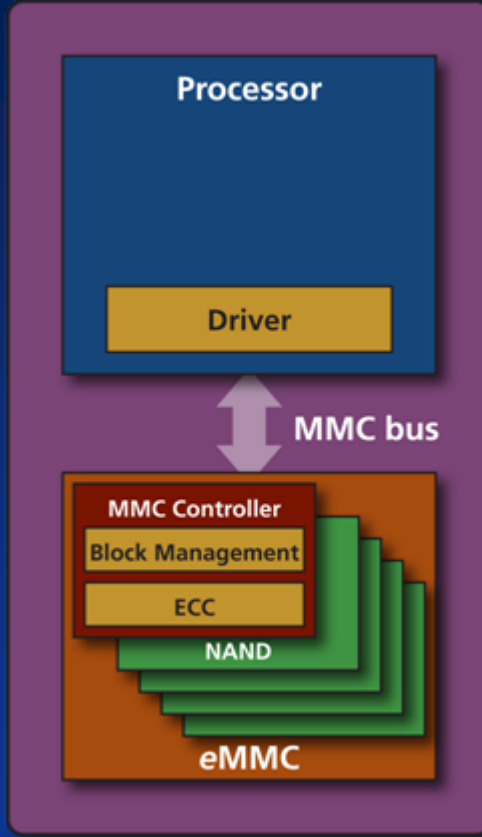
Raw vs. Managed Interface Examples

Direct NAND Interface



- Raw interface

MMC Interface



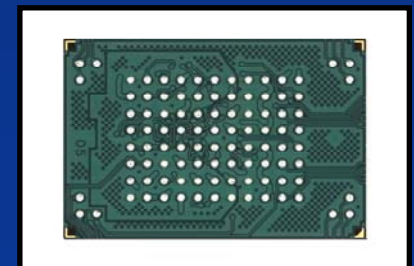
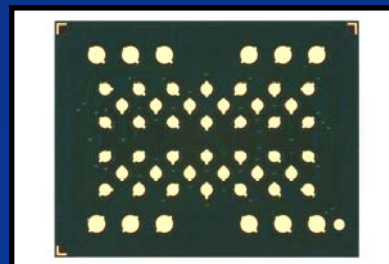
- Managed interface

Standard Raw and Managed Interfaces

- Raw
 - Asynchronous NAND
 - Source-synchronous NAND
- Managed
 - BA NAND
 - e-MMC
 - eSD
 - UFS

Open NAND Flash Interface (ONFI)

- Asynchronous NAND Flash interface
 - First defined in ONFI 1.0
 - Up to 50 MB/s interface
 - The ONFI 2.0 standard is backward compatible to ONFI 1.0
- Source-synchronous NAND Flash interface
 - Defined in ONFI 2.0
 - Up to 133 MB/s interface
 - Even faster interface speeds coming in ONFI 2.1



The ONFI Round-Up

- NAND consistencies with ONFI
 - Device identification using the parameter page
 - Array architecture and addressing
 - Command set
 - Timing modes and parameters
 - ECC and endurance
 - Factory-marked bad blocks
 - Device behavior and status
 - Packaging

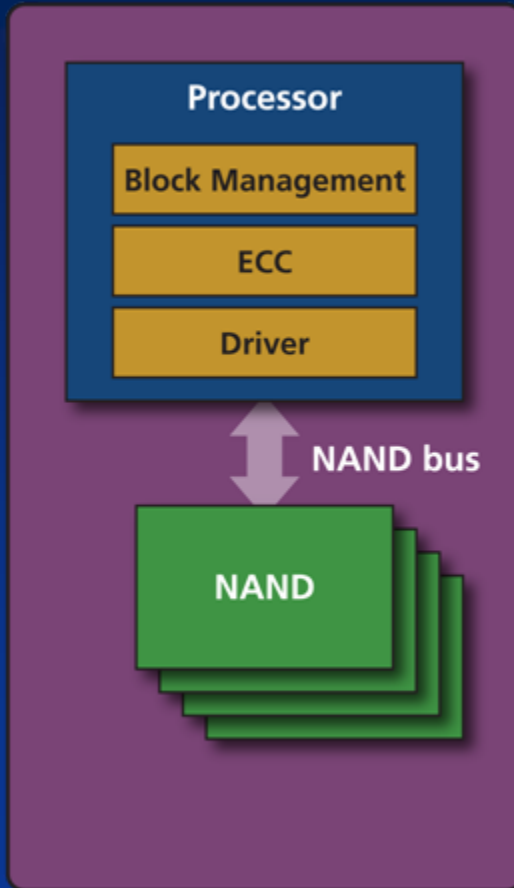
ONFI is a Standard, Not the Sheriff

- The ONFI specification does not mandate device architectures
 - Page size
 - Number of pages per block
 - Number of blocks
 - Number of planes
 - Amount of ECC required
 - Array performance

- They are discoverable by the host in the parameter page

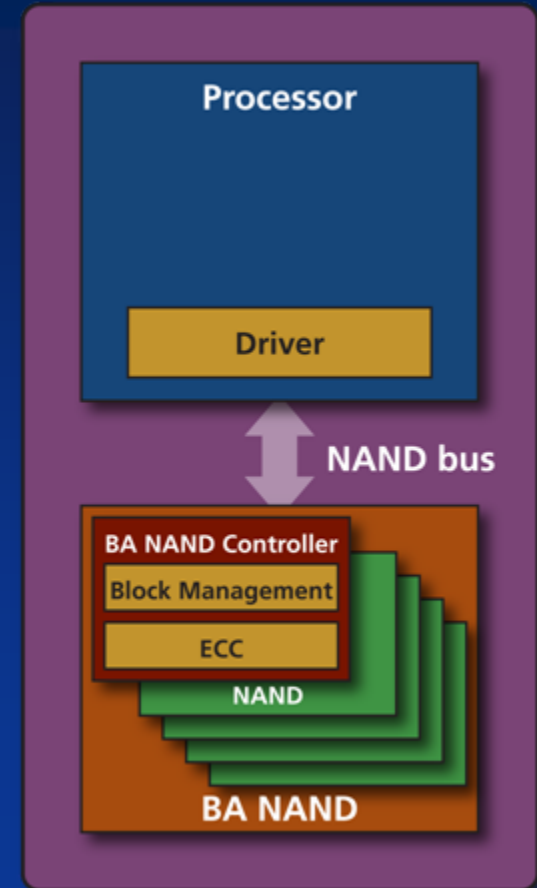
ONFI Block Abstracted NAND

Direct NAND Interface

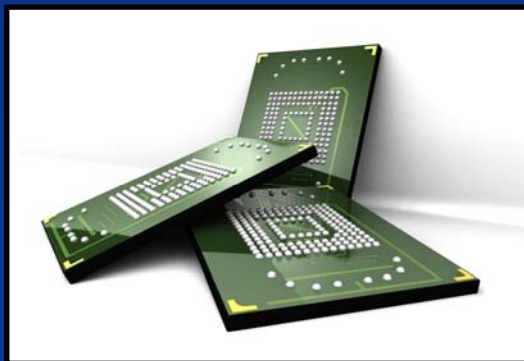


- BA NAND uses the same NAND interface (signals, electricals, packaging)
- Uses a different protocol
- Data is stored in sectors

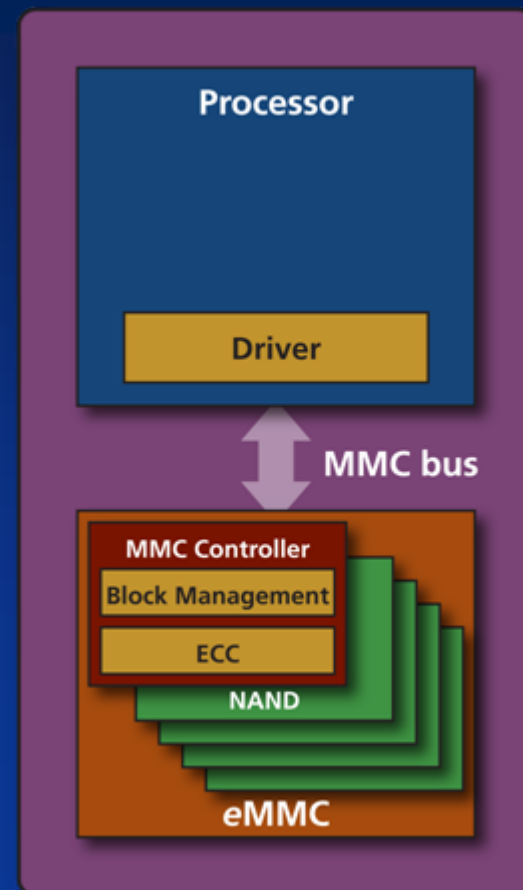
BA NAND Interface



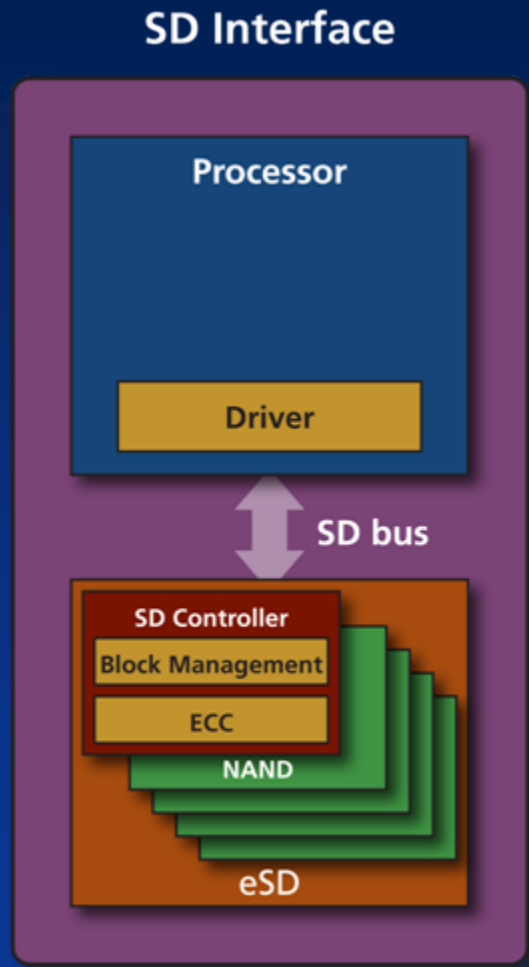
- Interface and packaging standardized by MMCA and JEDEC
- MMC interface found already on many wireless controllers today
- e-MMC is supported by most NAND vendors
 - Hynix (e-NAND)
 - Micron (e-MMC™)
 - Samsung (moviNAND™)
 - Toshiba (eMMC NAND)



MMC Interface



- Interface standardized by SDA; packaging compatible with JEDEC
- SD interface found already on many wireless controllers today
- Though a standard interface, it is not an open standard—not publicly published
- Not royalty-free





The interface “round-up”

Raw Interface Comparison

	Async NAND	Source-Sync NAND
Voltage	3.3V/1.8V	3.3V/1.8V
Data bus width	X8, x16	x8
Max clock	50 MHz	66 MHz DDR
Max transfer rate	50 MB/s	133 MB/s
Annual membership cost	None	None
Supplier support	Hynix Intel Micron	Intel Micron more coming...
Package standard	JEDEC/ONFI	ONFI

*TSOP package references JEDEC mechanical drawings.

Managed Interface Comparison

	BA NAND	eSD	e-MMC
Voltage	3.3V/1.8V	3.3V/1.8V	3.3V/1.8V
Data bus width	x8	x1, x4	x1, x4, x8
Max clock	50 MHz	50 MHz	52MHz
Max transfer rate	50 MB/s	25 MB/s	52 MB/s
Annual membership cost	None	Yes	None
Supplier support	Coming	Toshiba (eSD) Sandisk (iNAND)	Micron (e-MMC™) Samsung (moviNAND™) Toshiba (eMMC) Hynix (e-NAND)
Package standard	ONFI	JEDEC	JEDEC

*Follows JEDEC JC64.1 NAND card/module package format.

Upcoming Managed Interfaces

- UFS (JEDEC)
 - Uses ring topology for data transmission
 - Low voltage, high performance
 - One-to-many differential pairs for scalable throughput
 - Protocol optimized for storage interfaces

- USB 3.0 (USB-IF)
 - USB 3.0 controller may become embedded with NAND memory in the same package
 - Low voltage, high performance
 - One differential pair
 - Protocol optimized for many interfaces

Embedded Flash-Based Interface Standards Organizations

- MultiMediaCard Association (MMCA)
<http://www.mmca.org/>
- JEDEC
<http://www.jedec.org/>
- Open NAND Flash Interface (ONFI) Workgroup
<http://www.onfi.org/>
- SD Card Association (SDA)
<http://www.sdcard.org/>
- USB Implementers Forum
<http://www.usb.org/>

About Michael Abraham

- Manager of Micron's NAND Flash Applications Engineering group
- B.S. in Computer Engineering from Brigham Young University
- Micron's technical representative in ONFI and JEDEC for NAND Flash
- Key role in defining and standardizing the new high-speed NAND interface within Micron and at ONFI



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