

Technical Note

CellularRAM™ Asynchronous and Mixed-Mode Slow-Clock or Long-Setup WRITE Concerns

Introduction

CellularRAM™ devices support the industry-standard SRAM control bus, using CE#, OE#, WE#, and LB#/UB# for standard asynchronous read and write access. CellularRAM devices also support burst access by including the CLK, ADV#, and WAIT control balls associated with the industry-standard burst Flash interface.

This technical note highlights unique characteristics of CellularRAM WRITE cycles during asynchronous or mixed-mode operations at slow clock speeds or with long setup times.

CellularRAM Modes of Operation

The bus configuration register (BCR) defines the operational mode (either asynchronous or burst) and the specific configurations when burst mode is selected.

When burst mode is selected, a combination of synchronous READ operations and asynchronous READ and WRITE operations can be executed. This mode is referred to as mixed-mode (NOR Flash) operation. Mixed-mode asynchronous READ and WRITE operations require the clock (CLK) to remain static (LOW) for the entire sequence.

ADV# can be used to latch the target address, or it can remain LOW during the entire WRITE operation. For additional mixed-mode operational details, refer to the current part data sheet, available on Micron's CellRAM Web site (<http://www.micron.com/products/psram/cellularram/>).

Operation Clarification

Historically, asynchronous SRAM READ and WRITE cycles have been defined by cycle completion rather than cycle initiation. Such ambiguity can lead to unexpected behavior if the device operation is not fully understood and a WRITE cycle is aborted.

Moreover, CellularRAM burst mode operations with clock rates below 50 MHz can be interpreted by the device as a mixed-mode asynchronous access. Clock rates below 50 MHz are allowed as long as the time from the beginning of the burst read or write (initiated by the last CE# or ADV# LOW) to an active clock edge does not exceed 20ns. If this requirement is not met, an asynchronous operation is initiated.

When CE# goes LOW prior to an active clock edge, any address change or ADV# LOW event will abort the present access and initiate a new access. The start of an asynchronous access is defined here as the last of CE# LOW, any address change, or an ADV# LOW event. CLK must be held static LOW and OE# must be LOW to output data.

Unexpected Asynchronous WRITE

If the device is being operated in mixed-mode and t_{CSP} exceeds 20ns, then an asynchronous READ or WRITE will occur prior to the expected burst READ or WRITE.

For a READ operation, the user can expect to ignore the output from the asynchronous READ. The same data will be read again after the initial latency of the burst access has been reached.

For a WRITE operation, if the address and LB#/UB# have not changed between the asynchronous WRITE and the burst WRITE, the addressed location will simply be written again with the burst data. Care must be taken that t_{AS} (address and ADV# low setup time) is not violated, or an unexpected write will occur to the address present prior to that event.

See Figure 1 on page 3 for a visual representation of these processes.

t_{WI} : Time WRITE Invalid

A second possible issue relates to t_{WI} (time WRITE invalid) delay. As previously defined, an asynchronous cycle is initiated by an address change or a CE# or ADV# LOW event. A refresh opportunity is inherent in the CellularRAM operation at the beginning of each asynchronous cycle. During this time, the state of WE# will be ignored. This delay is referred to as t_{WI} (time WRITE invalid). If WE# were to go LOW and return HIGH during the t_{WI} delay, the WRITE operation would be ignored. To ensure that a WRITE operation is executed, the user must ensure that WE# is LOW at the beginning of the cycle or that WE# stays LOW longer than t_{WI} (20ns; see Figure 2 on page 4).

Figure 1: Unintended Asynchronous WRITE Preceding a Burst WRITE

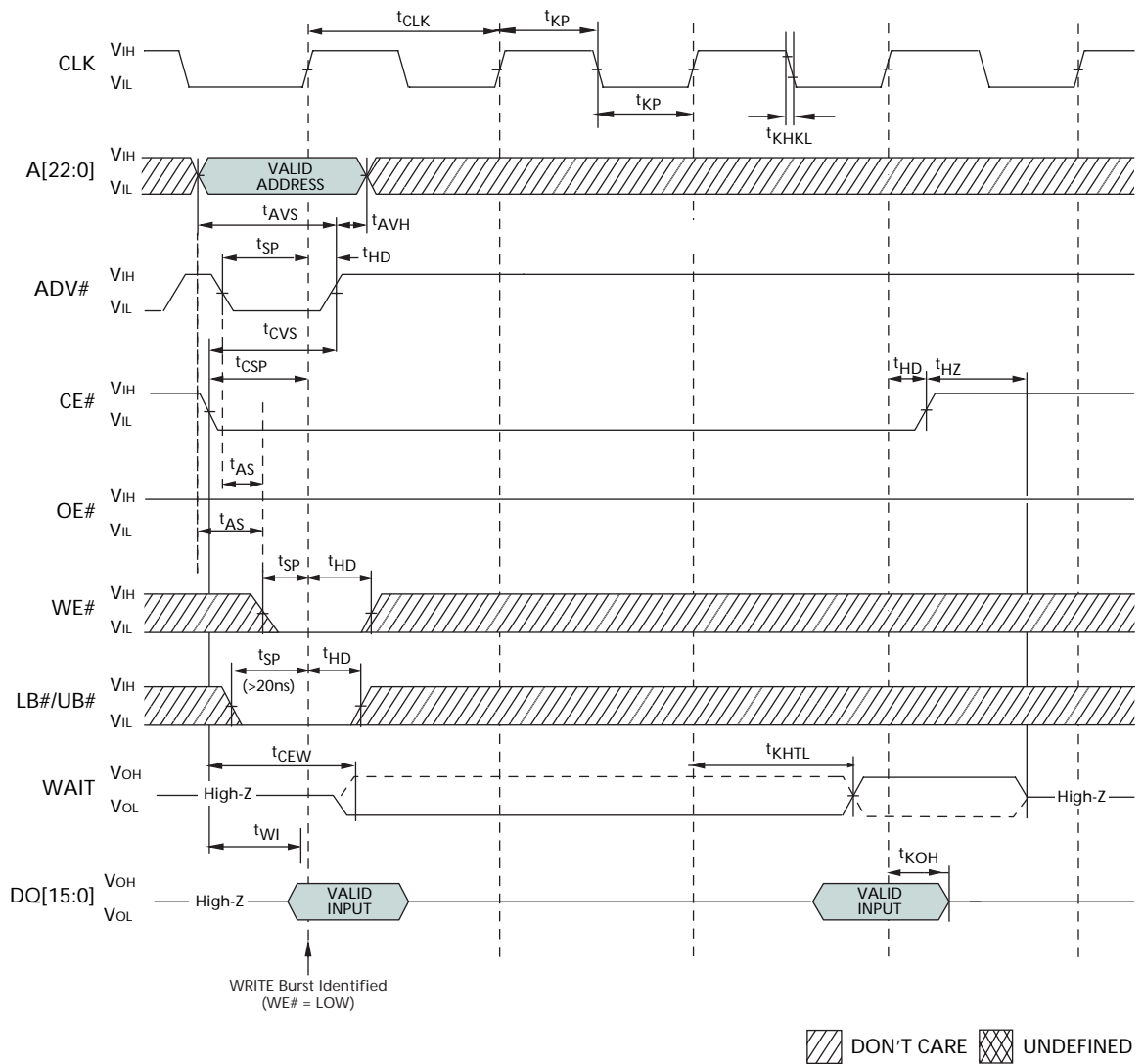
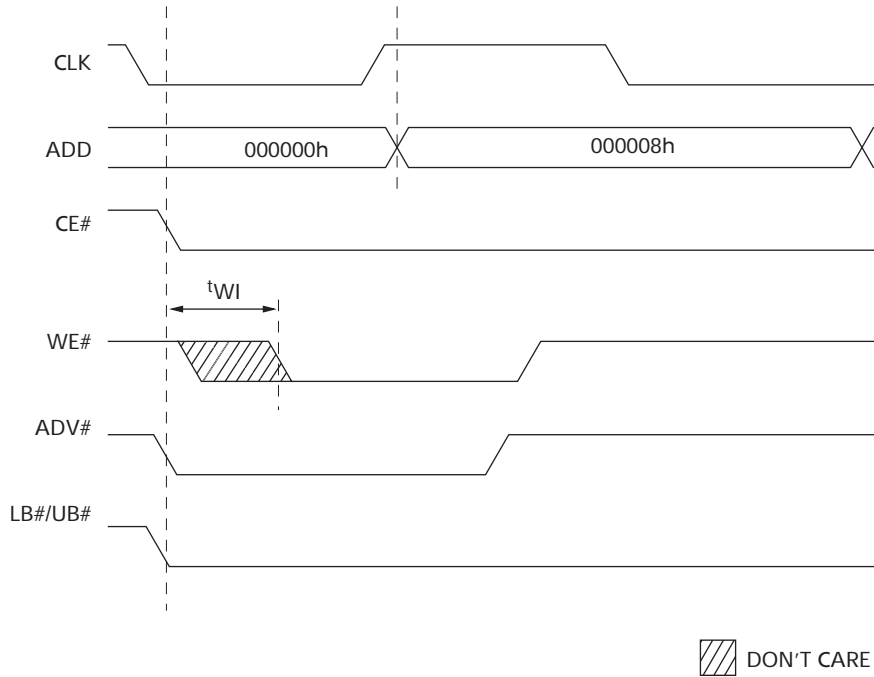


Figure 2: Time-Write-Invalid



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