

Technical Note

Density Migration for x16 Burst Multiplexed PSRAM Die

Introduction

The Micron[®] family of PSRAM devices is offered in several densities and in the following options: async/page, async/page/burst, and x16 burst multiplexed.

Micron also offers devices based on the CellularRAM Workgroup (www.cellular-ram.com) defined specifications. Therefore, the Micron family of PSRAM devices can be considered a superset of these specifications.

This technical note describes hardware and software considerations that need to be accounted for when migrating x16, burst multiplexed PSRAM-based designs from 16Mb to 64Mb.

The technical note provides:

- An overview of x16 burst multiplexed mode
- Device driver considerations
- Hardware considerations

Three PSRAM parts are discussed in this technical note:

- 16Mb, x16 burst multiplexed – MT45W1MW16MBP23Z
- 32Mb, x16 burst multiplexed – MT45W2MW16MBP24A
- 64Mb, x16 burst multiplexed – MT45W4MW16MBP25Z.

Data sheets for these parts are available on the Micron die Web page: www.micron.com/baredie/.

Burst Multiplex Overview

Basic PSRAM operation is the same in burst multiplexed mode as it is in non-burst multiplexed mode; the same control signals and timings apply to both operational modes. The only exception is that a x16 burst multiplexed device cannot work in page mode because the address inputs are used for the data bus and, therefore, will not allow for consecutive page addresses to be presented to the device address pads. The operation flow of the device to start a burst or async cycle is no different between the two styles of device, though the state of the DQ pads must be considered at all times.

Micron has three densities of x16 burst multiplexed PSRAM devices: 16Mb, 32Mb, and 64Mb, each of which derives from a different CellularRAM[™] generation. Because of this, the three densities require unique device driver and hardware considerations. Device drivers that support all densities need to account for subtle differences when migrating through the densities.

Micron x16, burst multiplexed devices are either CellularRAM 1.0- or 1.5-compliant, with the addition of multiplexed address and data lines.

Device Driver Considerations

The device driver is written to allow the memory controller to correctly interface with the PSRAM. The device driver controls the register settings needed for PSRAM operation.

Two configuration registers are available on PSRAM devices:

1. The bus configuration register (BCR)
2. The read configuration register (RCR)

Register Variations by Density

The two configuration registers, BCR and RCR, control numerous PSRAM device operations. The RCR operations are identical across all densities. BCR operations differ by density, as shown in Tables 1, 2, 3, and 4.

Table 1: BCR[2:0] – Burst Length

BCR[2]	BCR[1]	BCR[0]	Burst Length	Density Support
0	0	1	4 words	16Mb, 32Mb, 64Mb
0	1	0	8 words	16Mb, 32Mb, 64Mb
0	1	1	16 words	16Mb, 32Mb, 64Mb
1	0	0	32 words	64Mb only
1	1	1	Continuous	16Mb, 32Mb, 64Mb
Others			Reserved	–

Table 2: BCR[5:4] – Drive Strength

BCR[5]	BCR[4] ¹	Drive Strength ²	Density Support
0	0	Full	16Mb, 32Mb, 64Mb
0	1	1/2	64Mb only
1	0	1/4	16Mb, 32Mb, 64Mb
1	1	Reserved	–

- Notes: 1. BCR[4] is not supported and must be set to “0” on 16Mb/32Mb devices.
2. Full drive strength is the default on 16Mb/32Mb; 1/2 drive strength is the default on 64Mb.

Table 3: BCR[6]

BCR[6] Power-Up Default	Density	Notes
1	16Mb, 32Mb	Any value change will not affect device functionality. WRITE a “0” for density compatibility.
0	64Mb	As above.

Table 4: BCR[13:11] – Latency Codes

BCR[13]	BCR[12]	BCR[11]	Latency Counter	Density Support
0	0	0	Code 0	No support
0	0	1	Code 1	No support
0	1	0	Code 2	16Mb, 32Mb, 64Mb
0	1	1	Code 3	16Mb, 32Mb, 64Mb
1	0	0	Code 4	16Mb, 64Mb
1	0	1	Code 5	16Mb, 64Mb
1	1	0	Code 6	16Mb, 64Mb
1	1	1	Code 7	No support

Device ID Register (64Mb)

The device ID register (DIDR) is only supported on the 64Mb device. It is accessed by setting A[18] to “1” during a configuration register access. For the 16Mb/32Mb devices, A[18] must be set to “0” during all CRE-controlled register writes.

The DIDR register on the 64Mb device provides access to the information shown in Table 5:

Table 5: Device Identification Register Mapping

Bit Field	DIDR[15]	DIDR[14:11]		DIDR[10:8]	DIDR[7:5]	DIDR[4:0]
Field name	Row length	Device version		Device density	CellularRAM-compliant generation	Vendor ID
		Bit Setting	Version			
Bit setting	0b	0000b	1	010b	010b	00011b
		0001b	2			
Meaning	128 words			64Mb	CellularRAM 1.5	Micron

LB#/UB# Functionality

LB#/UB# functionality during burst READs differs for Micron’s burst A/D MUX devices, depending on whether the device design is CR1.0- or CR1.5-compliant. The 16Mb and 32Mb devices have a synchronous LB#/UB# input; the 64Mb devices have an asynchronous LB#/UB# input.

Hardware Considerations

Subtle differences exist between the densities. They are detailed in this section.

Pad Layout

The 16Mb and 32Mb devices offer identical pad ordering. The 64Mb device implements a unique pad ordering scheme.

Drive Strength

All of the devices support full (default) and half drive; the 16Mb and 32Mb devices also support quarter drive.

MAX Burst Speed

The 16Mb and 64Mb devices support 104 MHz; the 32Mb device supports 80 MHz.

Configuration Register Read (CRE operation)

The 64Mb devices support both CRE-enabled read and write configuration registers; the 16Mb and 32Mb devices only support a CRE-enabled write configuration register.

DIDR

The device ID register is available only on the 64Mb device.

Burst Write Wrap Length

The 16Mb and 32Mb devices support a continuous burst length for burst writes; the 64Mb device supports a write burst length identical to the burst read (via BCR[2:0]).

Burst Write Wrap Configuration

The 16Mb and 32Mb devices do not wrap within a burst length; the 64Mb density supports either wrapping within the burst length or a continuous burst.

Terminating a Burst

Burst termination by taking CE# HIGH is permitted across all densities. Burst termination with CE# LOW is available on the 64Mb device.

Deep Power-Down (DPD) Operation

All DPD entry and exit conditions are the same across the three densities. The 64Mb has an additional option for exiting DPD; the design can set CE# = LOW for 10 μ s.

Burst Length Options

All three densities support 4-, 8-, and 16-word and continuous burst operations. The 64Mb density also supports 32-word burst lengths.

Conclusion

As shown, the differences in devices cause some minimal variations in hardware and software considerations. Careful consideration of these differences will ensure that a controller will be able to support a x16 burst multiplexed PSRAM from 16Mb through 64Mb. For specifications on the devices, see the appropriate die data sheet, available at www.micron.com/baredie/, and for technical help, contact the PSRAM technical team via e-mail: at psramsupport@micron.com.



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Revision History

Rev. B	01/06
• Added LB#/UB# section	
Rev. A	11/05
• Initial release	