Technical Note

Implementing CellularRAM® 2.0 x32 with Two CellularRAM 1.5 x16 Devices

Introduction

Increasingly sophisticated mobile memory devices require the ability to store and retrieve large amounts of data. The need for operation at higher data rates, while maintaining a very small physical footprint, has lead Micron and other members of the CellularRAM Workgroup to introduce a CellularRAM® 2.0 (CR2.0) compliant line of x32 A/D MUX CellularRAM devices.

The purpose of this technical note is to document how the x32 CR2.0 memory interface can be emulated by using a two-die stack of x16 CR 1.5 devices. The solution presented in this technical note will allow early debug and evaluation of CR 2.0 compliant applications prior to the availability of "true" CR 2.0 devices.

Advantages of the CR 2.0 Specification

The CR 2.0 specification provides for high data rates, while reducing the number of device pins needed to support the memory interface. The CR 2.0 specification effectively doubles data rates by providing a 32-bit (x32) data bus. Micron plans on introducing CR 2.0 compliant devices early in 2006.

Designing chipsets that support a new memory interface is often delayed by the inability of vendors to provide working silicon as early as needed. Micron offers this stacked die solution to emulate the CR 2.0 device.

Data sheets for the CR 1.5 parts are available on the Micron die Web page:
http://www.micron.com/baredie/

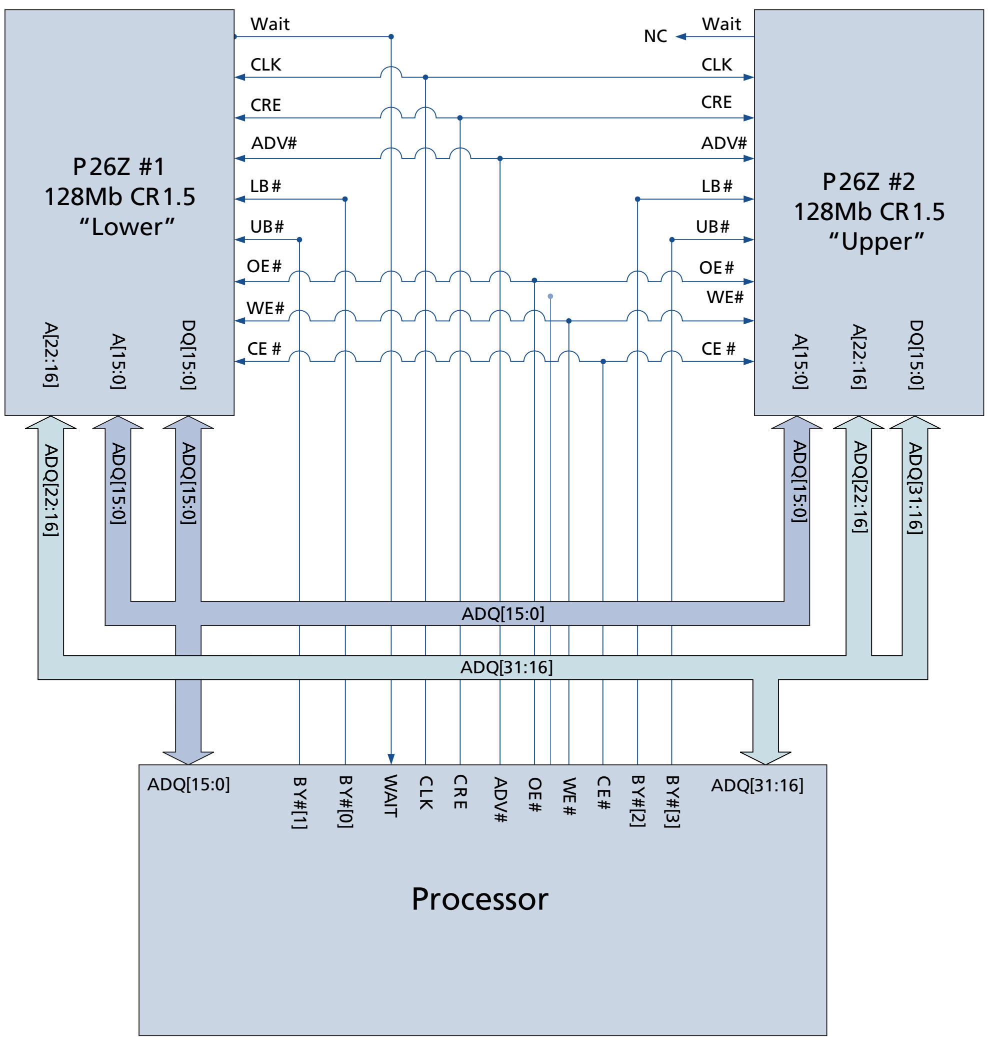
Connecting the Memory

To emulate the x32 CR 2.0 specification using two x16 CR 1.5 devices, various pins are shared between the memory devices and other pins are not. Table 1 lists the pin mapping required for this configuration. Figure 1 illustrates how the two-die stack should be connected.

Table 1: Pin Mappings Between Memory Devices

CR 2.0 Pad Name	CR 1.5 Die 1 Pad Name	CR 1.5 Die 2 Pad Name	Comments
A/DQ[15:0]	A[15:0] and DQ[15:0]	A[15:0]	
A/DQ[31:16]	A/DQ[22:16]	A[22:16] and DQ[15:0]	
BY#0	LB#	NC	
BY#1	UB#	NC	
BY#2	NC	LB#	
BY#3	NC	UB#	
Wait	Wait	NC	The wait pad on Die 2 is not connected.
CLK	CLK	CLK	
CRE	CRE	CRE	
ADV#	ADV#	ADV#	
OE#	OE#	OE#	
WE#	WE#	WE#	
CE#	CE#	CE#	

Figure 1: Interconnect Diagram of Two x16 CR 1.5 Devices



Limitations of the Two-Die CR 1.5 Implementation

Implementation of the CR 2.0 specification with two CR 1.5 devices results in several data sheet variations (DSVs). DSVs include functional or specification differences from the data sheet. Table 2 illustrates the DSVs that apply when using the two-die 1.5 implementation.

Table 2: DSVs for CR 2.0 and CR 1.5

Item	Data Sheet Variance	CR 2.0	CR 1.5 Implementation	Work-Around
1	Default mode on power-up	Burst	Async	BCR must be written to configure each device for burst operation[1].
2	Maximum clock rate	133 MHz	104 MHz	Run the memory clock at a slower rate.
3	Active currents	As listed in CR 2.0 data sheet	Isb, Ipar and Idpd ~2x CR 1.5 spec	No work-around.
4	A/DQ[31]	CRE and A/DQ[31] supported	CRE only available	Must use CRE or connect A/DQ [31] to CRE.
5	Fixed and variable latency modes	Supports both	Can only support fixed latency	Debug will only be possible in fixed latency mode.
6	DIDR density and generation	No issue	DIDR read will return CR 1.5 density and generation	The designer must be aware of the difference.
7	I/O capacitance	As listed in CR 2.0 data sheet	Higher than spec especially for A/DQ[22]	The designer must be aware of the difference.

NOTE:

1. Refer to the Hardware Access to the Configuration Registers section for more information.

Hardware Access to the Configuration Registers

Three variances from the CR 2.0 data sheet are worth including in this technical note. The first two variances impact hardware access to the configuration registers when the two-die stack is used.

1. The registers can be accessed using either a synchronous or an asynchronous operation when configuration enable (CRE) or A/DQ[31] is HIGH.

   In the case of this two-die stack, A/DQ[31] does not allow access to the configuration registers unless CRE is connected to A/DQ[31].

2. WRITEs to the BCR and RCR registers when using the two-die stack do not require any special software modifications to support CR 2.0.

   When reading the BCR, RCR, or DIDR of the two-die stack, however, the controller will be presented configuration register data from the lower die on A/DQ[15:0] and configuration data from the upper die on A/DQ[31:16]. The controller can ignore the data presented on A/DQ[31:16] (from the upper half of the memory).

Software Access to the Configuration Registers

The third DSV concerns the software access command sequence to READ or WRITE the configuration registers. This sequence requires that the OPCODE or register definition be presented to the CR 1.5 devices on the DQ bus. To allow both the upper and lower devices to be configured identically, the OPCODE must be presented to both the upper and lower devices by repeating the A/DQ[15:0] code on A/DQ[31:16]. The register read will be present for the lower die on A/DQ[15:0] and for the upper die on A/DQ[31:16] when initiating a software access READ of the configuration registers.

Conclusion

Chipset implementation and debug of a new interface specification requires compliant memory devices.

Micron is providing to customers a two-die stack that emulates the CR 2.0 specification prior to the availability of true CR 2.0 compliant silicon. This two-die stack effectively doubles data rates and reduces the number of pins needed to support the memory interface.

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Revision History

Rev. B 9/06

Row size difference item (previously row 6) was removed from Table 2 on page 3

Rev. A 11/05

- Initial release