

Technical Note

Designing Applications with the x16 Burst A/D Multiplexed Interface

Introduction

Today's mobile memory devices need to store and retrieve large amounts of data. Because operating at higher data rates while maintaining a very small physical footprint had become increasingly important, Micron introduces a line of Burst A/D multiplexed PSRAM devices. These PSRAM devices provide the same data rates as the CellularRAM 1.0 and 1.5 specifications, while reducing the number of device pins needed to support the memory interface.

This technical note provides guidance for designing applications that support the Burst A/D multiplexed interface. It discusses the A/D multiplexed interface and compares the A/D multiplexed interface to the standard burst interface for PSRAM. This technical note also details the benefits of the Burst A/D multiplexed interface.

Address and Data Multiplexed Interface

Memory devices that utilize an Address and Data multiplexed interface are commonly referred to as "A/D multiplexed" devices. Micron has taken the traditional Asynchronous A/D multiplexed interface one step further by providing Burst READ and WRITE capability.

To utilize the Burst A/D multiplexed interface, the system must support:

- Address and Data multiplexed Bus
- Control pins for Burst operation

Standard Burst PSRAM Interface

In Figure 1, the "Standard Burst" diagram illustrates the interface popularized by the CellularRAM Work Group in the CR1.0 and CR1.5 generations of the specification. The standard burst interface has separate Address and Data buses. The control pins needed for Asynchronous, Page, and Burst operation are: CE#, OE#, WE#, LB#, UB# CRE, CLK, ADV# and Wait.

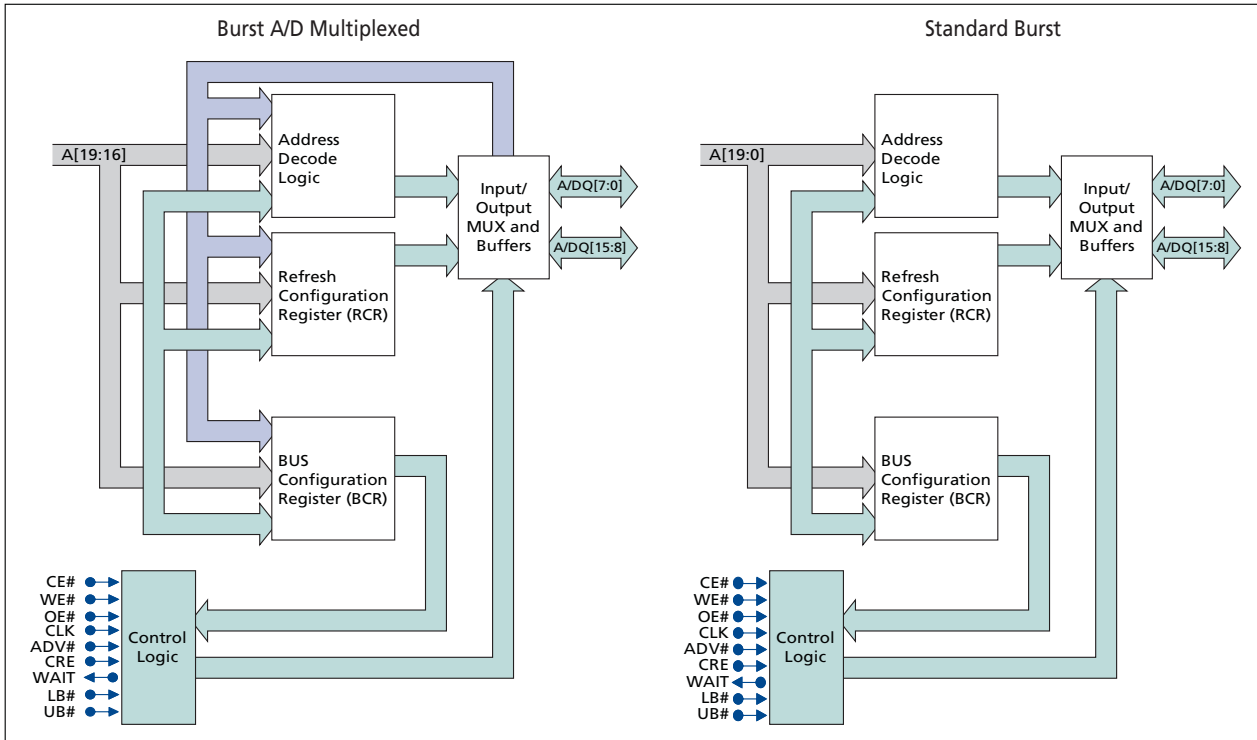
Burst A/D Multiplexed Interface

Figure 1 also illustrates the shared address and data bus required to implement the burst A/D multiplexed interface.

Page mode operation, as supported on the CellularRAM 1.0 and 1.5 specifications, is not supported for the A/D multiplexed interface.

No change in burst specifications is required when the A/D multiplexed interface is implemented. For a x16 104MHz CellularRAM device, data rates of approximately 208MB per second are possible with continuous burst READ or WRITE operations.

Figure 1: Burst A/D Multiplexed vs. the Standard Burst Interface



Burst A/D Multiplexed and Standard Burst Pad List Comparison

The burst A/D multiplexed interface is an appealing option for designs that require a decreased pin count. Decreasing the number of on-die connections simplifies the MCP substrate design, decreases the number of balls needed on the substrate, and simplifies the routing of the PC board. For Micron’s 16Mb device, the “Standard Burst” interface lists 71 pads of which 65 pads are bonded. In contrast, the “Burst A/D multiplexed” interface requires only 49 bonded pads, reducing the controller pin count by over 30%.¹

Conclusion

Designing applications with Burst A/D multiplexed devices provides standard Cellular-RAM performance with reduced pin count.

With the exception of Page mode support, no decrease in performance or features will be noted when designing with the Burst A/D multiplexed interface.

1. Controller pin count does not include power pins.



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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.