

Technical Note

Using CellularRAM™ to Replace UtRAM

Introduction

The Micron® family of CellularRAM™ devices is designed to be backward compatible with 6T SRAM and early-generation asynchronous and page PSRAM. Designs requiring high-speed and low-power operation constitute a major market segment where backward compatibility is essential. CellularRAM memory also provides a NOR Flash burst-compatible interface that allows designers to take their designs to the next performance level.

Samsung® Unit-transistor RAM (UtRAM™) competes in this market segment; this technical note addresses requirements for a design migration from Burst UtRAM to CellularRAM devices.

This technical note describes the following:

- Comparative device overview
- Interface-change requirements
- Device driver requirements
- Added benefits of using CellularRAM products

Table 1 shows an overview of comparative device features.

Table 1: UtRAM and CellularRAM differences

Function	UtRAM	Micron	Notes
Power-up time	200µs (MAX)	150µs (MIN)	Both default to Async mode
Page Mode Size	4-word	16-word	
Configuration Register - Interface type - Access allowed	Hardware ($\overline{\text{MRS}}$) only WRITE only	Hardware (CRE) and software WRITE and READ	
Burst Mode - Latency Type - Latency Codes	Fixed Only Latency Codes: 4–7	Both Variable and Fixed Latency Codes: 3–7	
Mixed mode Operation	Not supported	Supported	Clock stopped in Sync mode
WAIT pin - Active - Transition point	Burst READ and WRITE 1 clk before Data	Burst READ and WRITE 1 clk before or on clk edge	
PAR - Enabling point - Array Size	Only when part disabled Full, 1/4, 1/2 & 3/4	Once PAR setting accepted Full, 1/8, 1/4, 1/2 & None	
Low-Power options - Deep Power-Down - TCSR	Not supported Yes (< 40°C)	Supported Yes (full temp range)	

Device Overview

UtRAM

UtRAM devices were introduced by Samsung Electronics to satisfy market demand for a device that would, like Micron CellularRAM devices, integrate a high-speed core technology with a NOR Flash compatible interface.

UtRAM products are grouped as asynchronous-only and async/page/burst devices. Primary target applications are the mobile device market, including mobile phones/PDAs/DSCs. The main features are:

- Burst NOR Flash interface
- Independent addressing and data buses
- Support for Known Good Die (KGD) and packaged devices
- Hidden refresh control

This technical note focuses on the async/page/burst 128Mb UtRAM device, K1B2816B6M.

CellularRAM

Micron CellularRAM devices target applications similar to those targeted by UtRAM with the additional value proposition of the CellularRAM Work Group specification. This published common specification allows a designer to consider multiple sourcing.

CellularRAM memory, like UtRAM, is based on DRAM technology, supporting a high-speed memory interface, while meeting the additional requirement for low-power operating modes.

Features include:

- Support for 16Mb through 256Mb densities
- Small-package-footprint FBGA devices
- KGD devices
- Burst NOR Flash compatible interface
- Asynchronous, page, and high-speed (up to 133MHz) burst interface
- Low-power options including partial array refresh (PAR), low standby current, deep power-down (DPD) mode
- Hidden refresh control

This technical note focuses on the async/page/burst 128Mb CellularRAM Working Group, CRWG, CR1.5-compliant device, MT45W8MW16B.

Interface Change Requirements

This section covers the following:

- Power-up considerations and default operational mode
- Async/page mode differences
- Signal definitions
- Burst mode differences
- WAIT pin functionality
- Mode register set

Power-up Considerations and Default Operational Mode

Both the CellularRAM and UtRAM devices start their internal initialization phases when the power supply rail reaches a valid power supply level ($V_{CC} = 1.7V$). At this point, the internal control circuitry begins to initialize the internal control circuitry, and both devices will be available for the first access, $CE\# = LOW$, as described below:

Table 2: Initialization time

Device	Time	Default Mode
Micron	150 μ s (MAX)	Async
UtRAM	200 μ s (MIN)	Async

During this initialization phase, device configuration registers (CR) are loaded with their default values; the UtRAM device data sheet includes a comment stating that the contents of the UtRAM mode register is not guaranteed after power-up, and that a “Mode Register Set setting sequence is highly recommended.” Micron CellularRAM devices power up with working default values in the CR in all cases.

This means that Micron CellularRAM devices can work with both the time delay and CR setting sequence required for the UtRAM device.

Async/Page Mode Differences

Both devices support asynchronous mode (READ/WRITE) and page mode (READ) operations. The two differences in using the page mode READ interface are, firstly, the Micron device requires configuration via the refresh configuration register (RCR(7)) to enable this feature. When configured, the two devices work the same in this operating mode.

Secondly, the CellularRAM product supports 16-word page mode operation, compared with the 4-word size supported by the UtRAM device.

This means that the Micron device can be configured for page mode READ/async WRITE operation, as well as the UtRAM 4-word page limit. Users gain the added advantage of the larger CellularRAM design’s page size.

Signal Definitions

Signals are the same on both devices, with the exception of \overline{MRS} (UtRAM) and CRE (CellularRAM). The signals definitions vary as follows:

- Mode register set (\overline{MRS}) is used to interface with the mode register and enables partial array refresh (PAR).
- Configuration register enable (CRE) is the optional interface to the CR.

Later sections provide details regarding both the device mode register and low-power option settings.

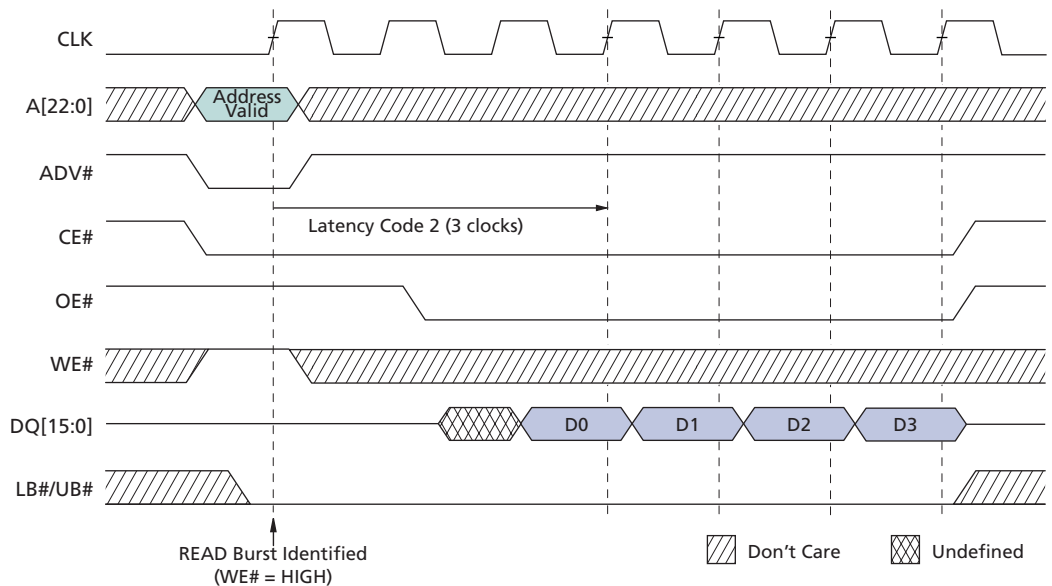
Burst Mode Differences

The UtRAM and CellularRAM devices both support the NOR Flash burst control interface (CLK/ADV# and WAIT) and the NOR Flash bus protocol. This support can be divided into the unique sections burst access and burst latency.

Identifying a Burst Access

Figure 1 shows a burst READ and the point at which the burst is identified. This point, the first active edge of CLK where ADV# is LOW, is also the point at which the address is latched and the burst 'latency' starts. This is the same for both the UtRAM and the CellularRAM devices. Although not shown, the burst WRITE operation is also identified at this point (WE# LOW).

Figure 1: Burst READ Timing



Burst Latency Codes

Table 3 defines the number of clocks until data is valid for a given latency code. The main difference between the two devices is that the Micron device uses the same latency code for both the burst READ and burst WRITE operations; for UtRAM, the burst WRITE latency is equal to (READ Latency – 1). This means that controller support for the burst function can be simplified; the point in the cycle where data is valid is consistent across all burst accesses.

Table 3: Latency Code Differences

	Latency (Clocks)	Notes
UtRAM	4–7	Fixed latency only
Micron	3–7	Variable and fixed latency

A controller that monitors WAIT can support the differences between the two devices without a noticeable impact in performance.

WAIT Pin Functionality

As with any burst interface, a signal is necessary to control the “throttling” of the interface between the master (memory controller) and the slave (memory) devices. The WAIT pin provides this function on both devices. The WAIT pin differences are detailed in the following section.

Note that unless detailed below, WAIT polarity and associated timings relative to activating/de-activating WAIT during a burst cycle are the same for both the UtRAM and CellularRAM devices.

WAIT Async/Page Operation

The UtRAM device documentation states that, “WAIT should be ignored during asynchronous operations.”

The Micron device will drive the WAIT pin during this operational mode but should be ignored as stated.

WAIT vs. Data Ready Driving (BCR(8))

The UtRAM device will always drive the WAIT# inactive for 1 clock cycle prior to when data is ready on a burst READ operation. The Micron device can be configured to match the UtRAM device or to drive WAIT inactive on the clock cycle where data is ready. This is configured via BCR(8).

By setting BCR(8) = 1, the two devices will work the same.

Mode Register Set ($\overline{\text{MRS}}$)

The UtRAM $\overline{\text{MRS}}$ input has two functions. One is to define the mode register settings; the other is to enable the partial array refresh (PAR) settings in the device.

Setting the Mode Register

To configure the options available in the UtRAM mode register, the design must drive the $\overline{\text{MRS}}$ signal active simultaneously with an asynchronous WRITE operation.

For the CellularRAM device, there are two options available for updating the CR: with hardware or software.

The hardware option is controlled via the CRE pin, which must be driven active HIGH to enable the CR configuration data presented on the address bus to be written into the appropriate CR. This operation can be performed with the CellularRAM device configured for either asynchronous or synchronous mode. All timings appropriate to the CR CRE-enabled asynchronous operation is compatible with the UtRAM mode register set operation. The CellularRAM device offers an option that exceeds the functionality of the UtRAM in the ability to READ the contents of the CRs.

The software option is not available with the UtRAM device and is therefore described in greater detail in a later section.

With a modification of the circuitry driving the $\overline{\text{MRS}}$ signal, i.e. inverting the signal to drive it ACTIVE HIGH, the Micron device can be used in place of the UtRAM device.

Enabling PAR

To enable the UtRAM PAR settings, the device must be disabled ($\text{CE}\#$ HIGH) while driving $\overline{\text{MRS}}$ ACTIVE LOW. This state will only continue while the part is disabled; any refresh occurring while $\overline{\text{MRS}}$ is HIGH will result in a full-array refresh.

The CellularRAM device does not require this two-stage operation. Once the PAR settings are enabled in the appropriate CR, via the RCR, then these PAR settings will be used any time a refresh is undertaken by the device. See “PAR” on page 7 for further discussion.

The CellularRAM PAR implementation functions with the noted implementation of the $\overline{\text{MRS}}$ signal, i.e. the PAR setting will already be enabled on the CellularRAM device; this combination of $\text{CRE}/\text{CE}\#$ does not affect CellularRAM device functionality.

Device Driver Changes

Previous sections discussed differences between UtRAM and CellularRAM devices in terms of hardware connectivity. Software differences between the two devices include the following areas:

- Burst options
- Access to the CRs
- Low-power configuration settings

Burst Options

As previously noted, some burst operation differences exist between the UtRAM and CellularRAM devices. The primary software differences are:

- Latency code programming to match the access time required by the memory controller for clock speed and the number of clock cycles to valid data
- WAIT polarity and valid drive strength options differences

Noted differences can be minimized by a memory controller supporting the appropriate WAIT pin functionality.

Access to the Mode Register/CRs

Although previously discussed, the modifications needed to support CRE instead of the $\overline{\text{MRS}}$ may require a device driver change, the input may be driven from a configurable output from the memory controller. If this is the case, this polarity change may require a change to the output definition.

Low-Power Configuration Settings

PAR

Both devices support the size reduction of the array that is actively refreshed, thus reducing refresh current consumption. This is called partial array refresh (PAR) in both the UtRAM and CellularRAM devices.

Although both devices support PAR, it must be emphasized that the setting changes in the CellularRAM device will take affect after the WRITE access to the RCR occurs. In the UtRAM device, it will only take affect when the \overline{MRS} input is active with CE# HIGH.

Deep Power-Down

The CellularRAM device supports an added feature whereby the lowest possible current consumption mode can be enabled. This feature requires a change to the software supporting the device; this is discussed in “Deep-Power Down” on page 9.

Feature Differences

Unsupported UtRAM Features

The only feature that cannot be supported on the CellularRAM device is interleaved burst mode. CellularRAM supports only linear burst mode.

CellularRAM Device Interface Improvements and Advantages

The CellularRAM device supports a variety of useful options for customer applications, including the capabilities listed below.

Configuration Register Access

READ and WRITE Access to the CRs

The CellularRAM device supports both READ and WRITE access to the three configuration registers on the device:

- Burst configuration register (BCR)
- Refresh configuration register (RCR)
- Device ID Register (DIDR)

The DIDR enables the designer to obtain information pertaining to the device they are accessing via software methods. Information such as manufacturer, device revision, and device density are available from this read-only register.

Software Access to the Configuration Registers

The three CellularRAM CRs can be accessed in a hardware or software initiated mode. The software method, that is not available on the UtRAM device, enables READ and WRITE access to the CR. The CellularRAM product data sheet contains the full definition of the interface; Table 4 gives an overview of the function. This function can be only performed in asynchronous operating mode.

Table 4: Software-Controlled Configuration Sequence (CellularRAM)

Cycle #	Operation	Address	Data
1	READ	MAX Address	X
2	READ	MAX Address	X
3	WRITE	MAX Address	Register select
4	WRITE READ	MAX Address MAX Address	Configuration value in Configuration value out

Latency – Variable or Fixed

The CellularRAM device supports both variable and fixed latency modes. Both latency modes offer benefits depending on memory controller requirements and interface.

Variable latency

Variable latency is the ability of a device to work at the highest performance levels via the WAIT pin and still maintain the ability to refresh as required. A pending refresh is signaled to the memory controller with the WAIT pin. If a refresh is required, the push-out—delay in the de-assertion—of the WAIT pin, only occurs after the refresh is complete. This push-out only occurs at the start of a cycle that has a refresh pending; on other cycles, the WAIT pin will not experience a push-out of the WAIT pin de-assertion.

Fixed latency

Fixed latency is provided to guarantee timing to the first access by enabling a refresh opportunity to occur at the start of every burst cycle. By providing a refresh opportunity, the first access is delayed by a defined period on both burst READs and WRITEs, thus eliminating the need to monitor the WAIT pin.

Burst Operation

Modes Supported

By using mixed-mode operation, the CellularRAM device supports any combination of burst and asynchronous READ or WRITE operations in synchronous mode (BCR(15) = 0).

The Micron device, via BCR(2:0), adds support for a burst length of 32 words. This is in addition to the standard 4-, 8-, and 16- word burst lengths and continuous burst mode.

The option is also provided to wrap or not wrap within a defined burst length using BCR(3).

Mode Switching

The UtRAM device data sheet contains a number of references to issues with mode switching from asynchronous to synchronous accesses, notably the possible corruption of the last WRITE access.

No known issues exist with the same mode switching on the CellularRAM device.

Burst Cycle Time

The UtRAM device requires that the burst cycle time (t_{BC}) must be $< 2.5\mu s$. The Micron CellularRAM device has the same requirement, t_{CEM} , but supports a maximum $4\mu s$.

Low-Power Options

Temperature-Compensated Self Refresh (TCSR)

Both the UtRAM and CellularRAM devices support TCSR via an on-board temperature sensor. The Micron device supports multiple internal TCSR settings up to, and including, 70°C whereas the UtRAM device only supports a maximum TCSR setting of 40°C.

This wider temperature range provides a major benefit in applications where devices are needed that must operate across the full supported temperature range of -40°C to +85°C.

Partial Array Refresh

The CellularRAM device gives customers more options when using PAR to reduce the refresh current by increasing the number of areas of the device that can be refreshed.

Deep-Power Down

The CellularRAM device is designed to operate in a mode where current consumption is targeted to be below the level shown for any of the PAR settings available with the UtRAM device. This option is enabled via RCR(4) and takes effect when the part is disabled, i.e., CE# is HIGH. When the deep power-down mode is selected (RCR[4] = 0), there will be a 150µs wake-up time required before CE# can be driven LOW.

Memory Block Diagrams

When replacing a UtRAM product with a CellularRAM product, it is necessary to understand the connections required between the memory controller and the memory devices (see Figures 2 and 3).

Figure 2: UtRAM Device Connection to Memory Controller

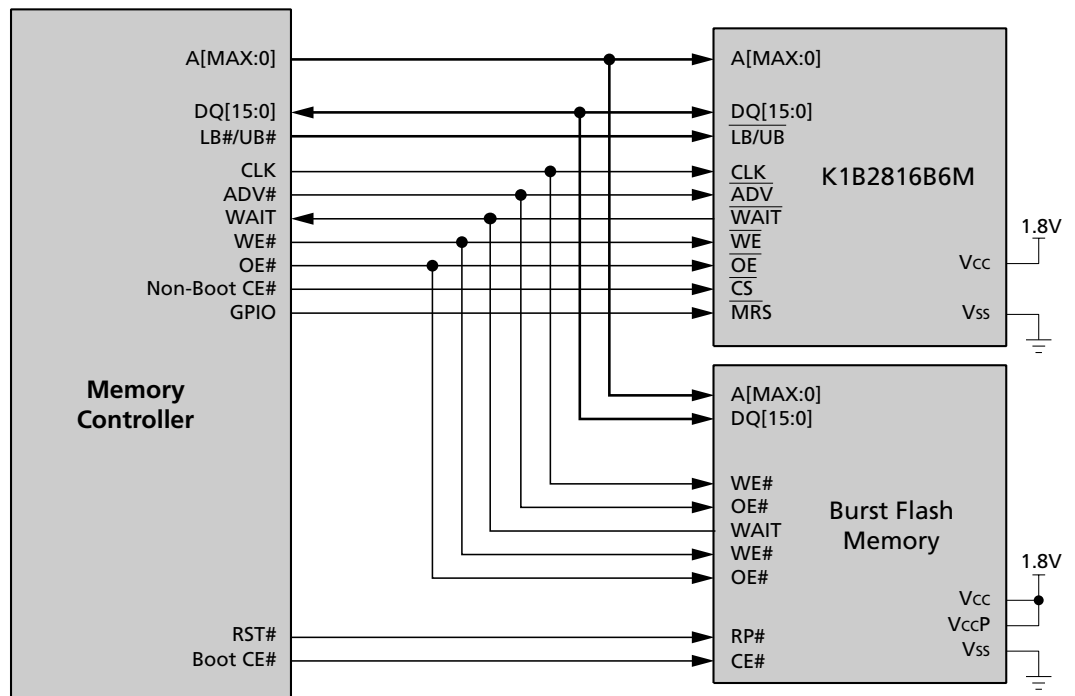
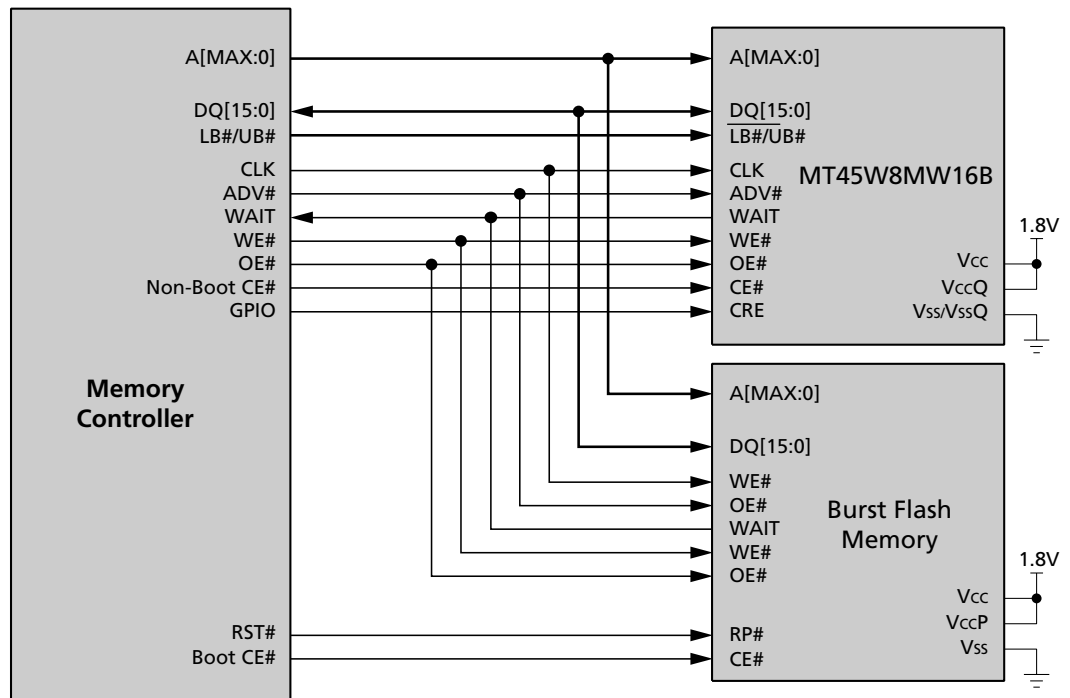


Figure 3: CellularRAM Device Connection to Memory Controller



Conclusion

The technical note shows areas of the current design that will need to be examined when considering the change to using Micron CellularRAM devices. These changes can be grouped together into the following areas:

- Configuring the CellularRAM
- Burst Latency configuration
- Memory Controller/CellularRAM device interface connections

For further technical assistance, e-mail psramsupport@micron.com or visit Micron's Web site: <http://www.micron.com/products/psram/>.

References

- Samsung UtRAM data sheet—K1B2816B6M (http://www.samsung.com/Products/Semiconductor/SRAM/UtRAM_PseudoSRAM/Synchronous/128Mbit/K1B2816B6M/ds_k1b2816b6m_rev10.pdf)
- Micron CellularRAM—MT45W8MW16B (http://download.micron.com/pdf/datasheets/psram/128mb_burst_cr1_5_p26z.pdf)



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Revision History

Rev. A	2/06
• Initial release	