

Technical Note

Using CellularRAM™ Memory to Replace Fujitsu 3V FCRAM

Introduction

Micron® CellularRAM™ devices are designed to be backward compatible with 6T SRAM and early-generation asynchronous and page PSRAM. Designs requiring high speed and low-power operation constitute one market segment where this backward-compatibility is essential. CellularRAM memory also provides an interface compatible with burst NOR Flash that allows designers to take their designs to the next performance level.

Fujitsu fast cycle random access memory (FCRAM) competes in this market segment. This technical note addresses requirements for a design migration from 3V FCRAM to CellularRAM devices.

This technical note describes the following:

- Comparative device overview
- Interface-change requirements
- Device driver requirements
- Added benefits of using CellularRAM memory

Table 1: 3V FCRAM and CellularRAM Differences

Function	3V FCRAM Device	Micron CellularRAM Device	Notes
Power-Up - Voltage range - Power-up time	2.6V–3.1V 300µs (MIN)	1.70V–1.95V 150µs (MAX)	Both default to asynchronous mode
Page Mode Size	8-word	16-word	
Configuration Register - Interface type - Access allowed	Software only WRITE only	Software and hardware (CRE) WRITE and READ	
Burst Mode - Latency type - Latency codes	Fixed only Latency codes: 3–5	Both variable and fixed Latency codes: 3–7	
Mixed Mode Operation	Not supported	Asynchronous or burst supported for asynchronous access	CLK stopped
WAIT Pin (during burst) - Active - Logic level - Transition point	Burst READ only Active LOW only 1 CLK before data	Burst READ and WRITE Active HIGH or LOW 1 CLK before or on CLK edge	
Partial Array Refresh (PAR) - Enabling point - Array size	Only when part disabled Full, 1/8, and 1/4	Once PAR setting accepted Full, 1/8, 1/4, 1/2, and None	
Low-Power options - Deep power-down - Temperature-compensated refresh (TCR)	Supported by sleep mode Not stated in data sheet	Supported Yes (full temperature range)	

Device Overview

FCRAM Devices

Fujitsu Electronics introduced FCRAM devices to satisfy market demand for a device that would, like Micron CellularRAM devices, integrate a high-speed core technology with a NOR Flash bus.

FCRAM products are async/page/burst devices. The primary target applications are the mobile device market, including mobile phones, PDAs, and digital still cameras. The main features are:

- Burst NOR Flash interface
- Independent addressing and data buses
- Support for known good die (KGD) and packaged devices

This technical note focuses on the 3V async/page/burst 128Mb FCRAM device, MB82DBR08163A.

CellularRAM Devices

Micron CellularRAM devices target applications similar to those targeted by 3V FCRAM with the additional value proposition of the CellularRAM Workgroup specification. This published common specification allows a designer to consider multiple sourcing.

CellularRAM memory, like FCRAM, is based on DRAM technology. It supports a high-speed memory interface, while meeting the additional requirement for low-power operating modes.

CellularRAM features include:

- Support for 16Mb through 256Mb densities
- Small-package-footprint FBGA devices
- KGD devices
- Burst NOR Flash compatible interface
- Asynchronous, page, and high-speed (up to 133 MHz) burst interface
- Low-power options including partial array refresh (PAR), low standby current, and deep power-down (DPD) mode
- Hidden refresh control

This technical note focuses on the async/page/burst 128Mb, CR1.5-compliant device, MT45W8MW16B.

Interface Change Requirements

This section covers the following topics:

- Power supply considerations
- Async/page mode differences
- Signal definitions
- Burst mode differences
- WAIT pin functionality
- Chip Enable (CE2) operation

Power Supply Considerations

Several differences exist between the power supply needs of the CellularRAM and 3V FCRAM devices.

Core and I/O Voltage Supply

The core voltage for the two devices differ; the CellularRAM device supports a 1.70V–1.95V range, while the 3V FCRAM device supports 2.6V–3.1V. The I/O voltage for the two devices is the same—only the design's core voltage must be changed to work with the CellularRAM device.

Device Initialization

Both CellularRAM and 3V FCRAM devices start their internal initialization phases when the core supply rail reaches a valid power level (FCRAM = 2.6V; CellularRAM = 1.7V). At this point, the internal control circuitry begins to initialize, and both devices will be available for the first access, CE# = LOW, as described below.

Table 2: Initialization Time

Device	Time	Default Mode
Micron CellularRAM	150μs (MAX)	Asynchronous
3V FCRAM	300μs (MIN)	Asynchronous

During this initialization phase, the device configuration registers (CR) are loaded with their default data sheet values; both the FCRAM and CellularRAM devices power up in a default asynchronous mode.

This means that the Micron device can work with the time delay and CR setting sequence required for the 3V FCRAM device with the exception of the different device power supply ranges.

Async/Page Mode Differences

Both devices support asynchronous mode (READ/WRITE) and page mode (READ) operations. There are two differences in using the page mode READ interface. First, the Micron device requires configuration via the refresh configuration register (RCR[7]) to enable this feature. When configured, the two devices work the same in this operating mode.

Second, the CellularRAM product supports 16-word page mode operation, compared to the 8-word size supported by the 3V FCRAM device.

This means that the Micron device can be configured for page mode READ/async WRITE operation, and is fully compatible with the FCRAM 8-word page limit. Users gain the advantage of the CellularRAM design's larger page size.

Signal Definitions

Signals are the same on both devices, with the exception of CE2 (3V FCRAM) and CRE (CellularRAM). The signals definitions vary as follows:

- Chip enable 2 (CE2) is used to enable partial array refresh (PAR) and sleep mode.
- Configuration register enable (CRE) is an optional interface to the CR.

Later sections provide details regarding both the device configuration register and low-power option settings.

Burst Mode Differences

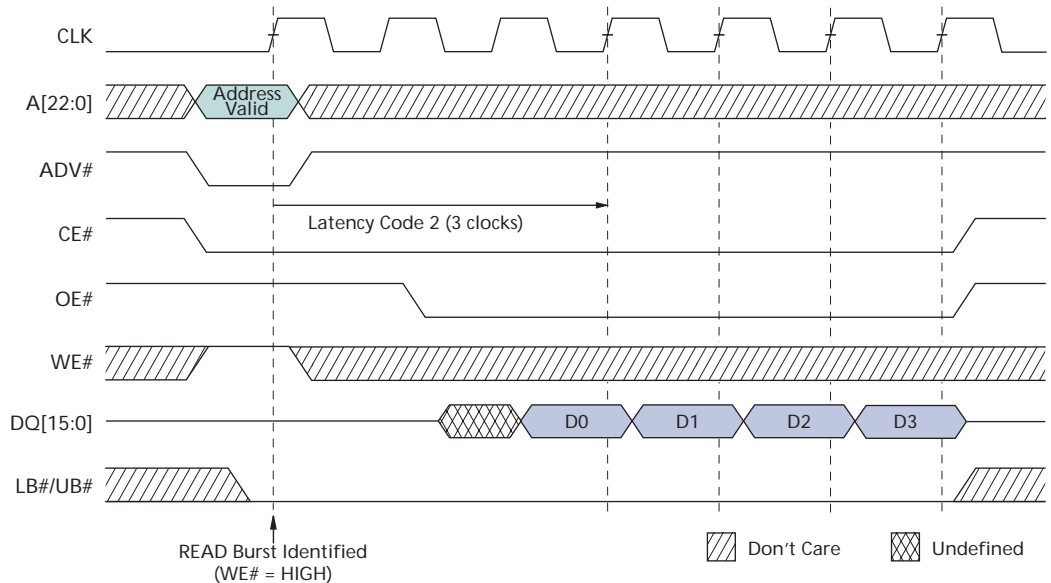
The CellularRAM and 3V FCRAM devices both support the NOR Flash burst control interface (CLK/ADV# and WAIT) and the NOR Flash command sequence. This support can be divided into the following unique sections.

Identifying a Burst Access

Figure 1 shows a burst READ and the point that the burst is identified. This point, the first active edge of CLK where ADV# is LOW, is also the point at which the address is latched and the burst “latency” starts. This is the same for both the FCRAM and the CellularRAM devices. Although not shown, the burst WRITE operation is also identified at this point (WE# LOW).

The state of WE# during the first rising CLK edge defines whether the operation is a READ or WRITE.

Figure 1: Burst READ Timing



Burst Latency Codes

Table 3 defines the number of clocks until the data is valid for a given latency code. The main difference between the two devices is that the Micron device uses the same latency code for both the burst READ and burst WRITE operations; for FCRAM, burst WRITE latency = (READ Latency - 1). This means that controller support for the burst function can be simplified.

Table 3: Latency Code Differences

Device	Latency (clocks)	Notes
3V FCRAM	3–5	Fixed latency only
Micron CellularRAM	3–7	Variable and fixed latency

It should also be noted that the value that is programmed into the CR differs between the CellularRAM and FCRAM devices. For the FCRAM device, the CR value—read latency (RL)—is defined as “the number of clock cycles between the address being latched and the first read data becoming available.” For the CellularRAM device, the CR value—latency count (LC)—is defined as “the number of clock cycles between the beginning of a READ or WRITE operation and the first data value transferred.” Therefore, the CellularRAM CR value should be programmed as $LC = (RL - 1)$.

A controller that monitors WAIT can support the differences between the two devices without a noticeable impact in performance.

WAIT Pin Functionality

As with any burst interface, a signal is necessary to control the “throttling” of the interface between the master (memory controller) and the slave (memory) devices. WAIT functions this way on both devices. The only support differences are detailed in the following section.

Note that all other WAIT polarity and associated timings relative to activating/deactivating WAIT during a burst cycle are the same for both devices.

WAIT Async/Page Operation

The 3V FCRAM device documentation states that, “ $\overline{\text{WAIT}}$ output is always in high impedance.”

The Micron device will drive WAIT during this operational mode, but should be ignored as stated.

WAIT Burst Operation

The 3V FCRAM device drives $\overline{\text{WAIT}}$ differently depending on whether it is in a burst READ or WRITE operation.

For an FCRAM burst READ $\overline{\text{WAIT}}$, output is driven LOW when the cycle starts and then will be driven HIGH one clock cycle before the data is ready. Once the burst completes, WAIT is driven High-Z.

An FCRAM burst WRITE $\overline{\text{WAIT}}$ output is driven HIGH when the cycle starts and remains at that level during the duration of the cycle. Once the burst completes, $\overline{\text{WAIT}}$ is driven High-Z.

The CellularRAM device drives WAIT “polarity” depending on the value in BCR[10] and is consistent across both burst READ and WRITE operations.

This means that the Micron device can work with the FCRAM WAIT functionality if WAIT is set for active LOW (BCR[10] = 0). Because this is not the default setting, it will need to be configured via the CR.

WAIT vs. Data Ready Driving (BCR[8])

The 3V FCRAM device will always drive $\overline{\text{WAIT}}$ to a deasserted state one clock cycle prior to when data is ready on a burst READ operation. The Micron device can be configured to match the FCRAM device or to drive WAIT to a deasserted state on the clock cycle where data is ready. This is configured via BCR[8].

By using BCR[8] = 1, the active level for the two devices can be configured the same.

Chip Enable (CE2) Operation

The 3V FCRAM CE2 input controls the enabling of the low-power settings: partial array refresh (PAR) and sleep mode. During normal operations this input must be active HIGH for the FCRAM to function correctly.

The equivalent input on the CellularRAM device, CRE, is only active (HIGH) during access to the configuration registers in hardware mode. For normal operations, this input must be held LOW, so a change to the device driver supporting the CE2 input will be required to support the CellularRAM device CRE input.

Enabling Partial Array Refresh

To enable the 3V FCRAM PAR settings, the device must be disabled ($\overline{\text{CE1}}$ HIGH) while CE2 is deasserted (LOW). This low-power PAR state will only continue while the part is disabled. Any refresh occurring while CE2 = HIGH will result in a full array refresh.

The CellularRAM device does not require this two-stage operation. Once the PAR settings are enabled in the appropriate CR, via the RCR, then these PAR settings will be used any time a refresh is undertaken by the device. See “Partial Array Refresh” on page 8 for further discussion.

The CellularRAM PAR implementation functions with the noted implementation of the CE2 signal. For example the PAR setting will already be enabled on the CellularRAM device. This combination of CRE/CE# does not affect CellularRAM device functionality.

Device Driver Changes

Previous sections discussed the differences between 3V FCRAM and CellularRAM devices in terms of hardware connectivity. The software differences between the two devices include the following areas:

- Burst options
- Access to the configuration registers
- CE2 functionality
- Low-power configuration settings

Burst Options

As previously noted, some burst operation differences exist between the 3V FCRAM and CellularRAM devices. The primary software differences are:

- Latency code programming to match the access time required by the memory controller for clock speed and the number of clock cycles to valid data.
- WAIT driving/polarity and valid drive strength options differences.

Noted differences can be minimized by a memory controller supporting the appropriate WAIT pin functionality.

Access to the Configuration Register

The 3V FCRAM device supports a six-cycle software sequence to setup the CR as detailed below.

Table 4: 3V FCRAM Configuration Sequence

Cycle #	Operation	Address	Data
1	Read	7FFFFFFh (MSB)	Read data (RDa)
2	Write	7FFFFFFh	RDa
3	Write	7FFFFFFh	RDa
4	Write	7FFFFFFh	X
5	Write	7FFFFFFh	X
6	Write	Address key	Read data (RDb)

This operational sequence is very close to the CellularRAM device four-cycle software sequence shown in Table 5 on page 7.

Table 5: Software-Controlled Configuration Sequence

Cycle #	Operation	Address	Data
1	READ	MAX address	X
2	READ	MAX address	X
3	WRITE	MAX address	Register select
4	WRITE READ	MAX address MAX address	Configuration value in Configuration value out

The CellularRAM device also offers other options to control the CR. These options are detailed in “CellularRAM Device Interface Improvements and Advantages” on page 8.

Overall, the software algorithm requires minimal changes to support software-enabled access to the CellularRAM device CRs.

CE2 Functionality

Although previously discussed, the modifications needed to support CRE instead of CE2 may require a device driver change, since the input may be driven from a configurable output from the memory controller. If this is the case, this polarity change may require a change to the output definition. In the alternative case, where CE2 is tied HIGH because the design does not use it, supporting the CellularRAM CRE input may require a PCB change, a software change, or both.

Low-Power Configuration Settings

Partial Array Refresh

Both devices support size reduction of the array that is being actively refreshed, thus reducing refresh current consumption. This is called partial array refresh (PAR) in both the 3V FCRAM and CellularRAM devices.

Although both devices support PAR, the setting changes in the CellularRAM device will take effect after the WRITE access to the RCR occurs. In the FCRAM device, these setting changes will only take effect when the CE2 input is LOW with $\overline{\text{CE1}}$ HIGH.

Deep Power-Down

Both devices support a feature whereby the lowest possible current consumption mode can be enabled. This mode, “sleep” (3V FCRAM) or “deep power-down” (CellularRAM), results in no refresh occurring on the array and allows the current consumption of the device to be in the 10 μ A range. To exit from this mode into normal operation, the system must support a “delay” to allow the device to initialize, see Table 2 on page 3.

Feature Differences

Unsupported 3V FCRAM Features

The only features that cannot be supported on the CellularRAM device are:

- Burst READ suspend support via the control of OE# during the cycle (the CellularRAM device can support Burst READ suspend operations by stopping the active CLK)
- Burst WRITE suspend support via the control of WE# during the cycle
- Software access to the configuration register is limited to asynchronous operating mode only
- Burst READ/single WRITE support via the configuration register (the CellularRAM device supports either a full burst or asynchronous access)

CellularRAM Device Interface Improvements and Advantages

CellularRAM devices support a variety of useful options for customer applications, including the capabilities listed below:

- Configuration register access
- Latency modes
- Burst operation
- Low-power options

Configuration Register Access

READ and WRITE Access to the Configuration Registers

The CellularRAM device supports both READ and WRITE access to the three configuration registers on the device:

- Burst configuration register (BCR)
- Refresh configuration register (RCR)
- Device ID register (DIDR)

The DIDR enables the designer to obtain information pertaining to the device they are accessing via software methods. Information such as manufacturer, device revision, and device density are available from this read-only register.

Hardware Access to the Configuration Registers

The three CellularRAM configuration registers can be accessed in a hardware- or software-initiated mode. The hardware method, not available on the 3V FCRAM device, enables READ and WRITE access to the CR. The CellularRAM data sheet contains the full definition of this interface.

This function can be performed in both asynchronous and synchronous operating modes.

Configuration Register Default Values

When reconfiguring the CellularRAM device for asynchronous operation ($BCR[15] = 1$), the device driver must only change the required BCR settings. All other BCR values can be left unchanged, as they will be ignored.

The 3V FCRAM data sheet states that, "Except for PS, all the other key inputs must be '1.'" When the FCRAM is configured for asynchronous operation ($M = 1$), all other configuration values must be "1."

Latency—Variable or Fixed

The CellularRAM device supports both variable and fixed latency modes. Both latency modes offer benefits that depend on memory controller requirements and the CellularRAM device interface.

Variable Latency

Variable latency is the ability of a device to work at the highest performance levels via WAIT and still maintain the ability to refresh as required. A pending refresh is signaled to the memory controller with WAIT. If a refresh is required, the push-out delay in the de-assertion of WAIT only occurs after the refresh is complete. This push-out only occurs at the start of a cycle that has a refresh pending; on other cycles, WAIT will not experience a push-out of WAIT de-assertion.

Fixed Latency

Fixed latency is provided to guarantee timing to the first access by enabling a refresh opportunity at the start of every burst cycle. By providing a refresh opportunity, the first access is delayed by a defined period on both burst READs and WRITEs, thus eliminating the need to monitor WAIT.

Burst Operation

Modes Supported

By using mixed-mode operation, the CellularRAM device supports any combination of burst and asynchronous READ or WRITE operations in synchronous mode ($BCR[15] = 0$).

The Micron device adds support for a burst length of 32 words via $BCR[2:0]$. This is in addition to the standard 4-, 8-, and 16-word burst lengths and continuous burst modes.

An option is also provided to wrap or not wrap within a defined burst length using $BCR[3]$.

Mixed Mode Operation

The ability of a device to switch between synchronous and asynchronous operational modes is called “mixed mode.”

Mixed mode operation with a 3V FCRAM design requires the software driver to switch modes, reconfiguring the CR from synchronous to asynchronous operation via the mode register (M[A15]).

Mixed mode operation with a Micron CellularRAM design is much easier, since the CellularRAM device allows the design to remain configured for synchronous mode operation, BCR[15] = 0. In this mode, the CellularRAM device can operate in the asynchronous mode by just stopping the CLK input. This simplifies the device driver and allows the device to stay configured for synchronous mode.

Low-Power Options

Temperature-Compensated Refresh (TCR)

The CellularRAM device supports TCR with the support for multiple internal TCR settings across the supported device temperature range. This ensures that the refresh rate is adjusted according to the operating temperature.

Partial Array Refresh (PAR)

The CellularRAM device gives customers more options when using PAR to reduce the refresh current by increasing the number of areas of the device that can be refreshed.

Deep Power-Down (DPD)

The CellularRAM device gives customers better control when enabling deep power-down mode. This mode, as mentioned previously, is the same as the 3V FCRAM “sleep mode,” but splitting the CellularRAM PAR and DPD registers from the other burst options provides greater flexibility for the designer.

Memory Block Diagrams

When replacing a 3V FCRAM product with a CellularRAM product, it is necessary to understand the connections required between the memory controller and the CellularRAM device (see Figures 2 and 3).

Figure 2: 3V FCRAM Device Connection to Memory Controller

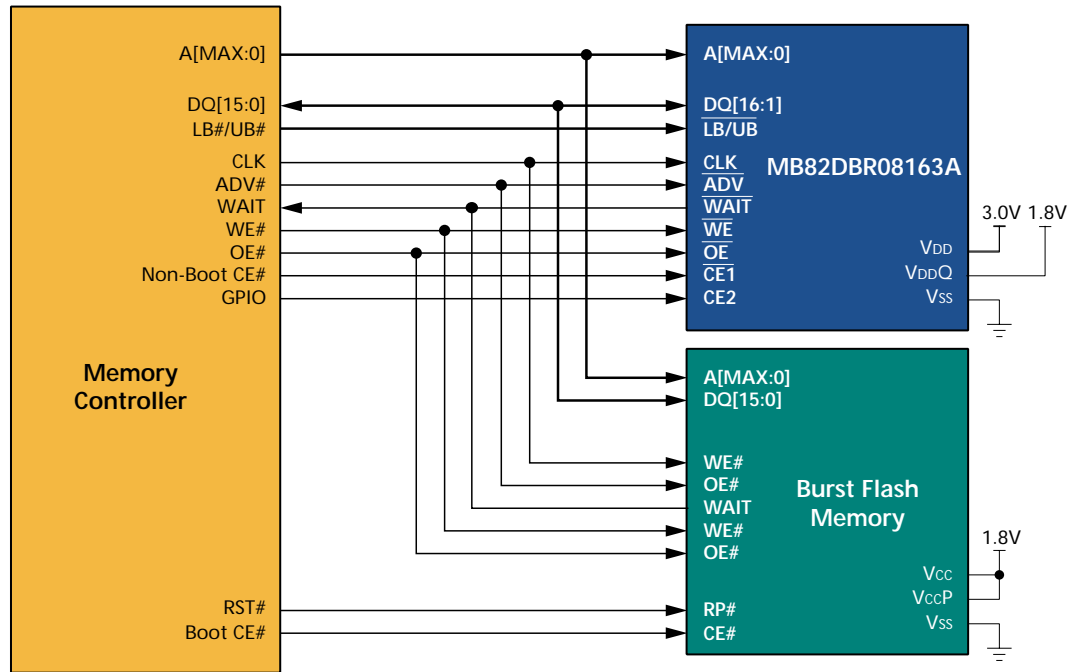
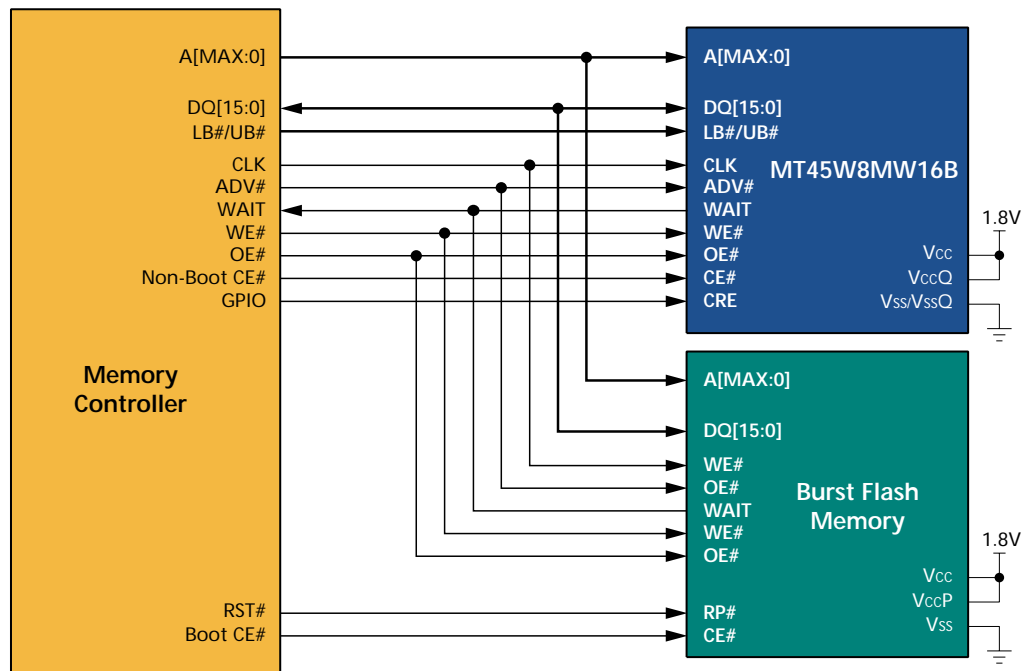


Figure 3: CellularRAM Device Connection to Memory Controller



Conclusion

This technical note shows areas of the current design that must be examined when considering a transition to Micron CellularRAM devices. These changes can be grouped together into the following areas:

- Configuring the CellularRAM device
- Burst latency configuration
- Memory controller/CellularRAM device interface connections

For further technical assistance, e-mail psramsupport@micron.com or visit Micron's Web site: www.micron.com/products/psram.

References

- Fujitsu 3V FCRAM data sheet—MB82DBR08163A
www.fujitsu.com/global/services/microelectronics/product/memory/fcram
- Micron CellularRAM data sheet—MT45W8MW16B
www.micron.com/products/psram/cellularram



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Revision History

Rev. 1.0	2/06
<ul style="list-style-type: none">• Initial release	