

# Technical Note

## Using CellularRAM™ Memory to Replace Single- and Dual-Chip Select SRAM

### Introduction

Micron® CellularRAM™ devices are designed to be backward-compatible with 6T SRAM and early-generation asynchronous and page PSRAM. Designs that require high speed and low-power operation make this sort of backward-compatibility essential. CellularRAM memory also provides an interface compatible with burst NOR Flash, which allows increased design performance.

This technical note discusses the changes required to convert single- or dual-chip select (CE#) SRAM to Micron CellularRAM memory. The following areas will be covered:

- Comparative device overview
- Power supply considerations
- Memory controller interface
- Low-power settings
- Package changes
- Added benefits of using CellularRAM memory

### Comparative Device Overview

Table 1 shows an overview of comparative device features.

**Table 1: SRAM and CellularRAM Memory Feature Differences**

Function	SRAM		Micron CellularRAM Memory	Notes
	Single CE#	Dual CE#		
Voltage – Core – I/O	Various 1.65–1.95V	Various 1.65–1.95V	1.70–1.95V 1.70–3.30V	I/O voltage must match
Operation Mode – Async READ/WRITE – Access time – Page	Yes 70ns No	Yes 70ns No	Yes 70ns Yes	
Low Power Support – Hardware control – Software control	Yes No	Yes No	Yes Yes	
Package	TSOP/FBGA	TSOP/FBGA	48-ball VFBGA	

## SRAM Devices

Various manufacturers produce SRAM devices that have either a single- or dual-CE# interface, which provides different feature support. All SRAM have an asynchronous interface with the memory controller and offer READ, WRITE, and data-retention modes.

## CellularRAM Devices

Micron CellularRAM devices target similar applications as SRAM, but offer the additional value of the CellularRAM Workgroup specification—a common, published specification that allows designers to consider multiple part vendors.

CellularRAM memory is based on DRAM technology. It supports a high-speed memory interface while meeting the additional requirement for low-power operating modes.

CellularRAM device features include:

- 16Mb–128Mb densities
- Small-footprint VFPGA package or known-good die (KGD)
- Burst NOR Flash-compatible interface
- Asynchronous, page, and high-speed (up to 133 MHz) burst interface
- Low-power options including partial-array refresh (PAR), low standby current, and deep power-down (DPD)
- Temperature-compensated refresh (TCR)
- Hidden refresh control

This technical note compares Micron's async/page 16Mb, CR1.0-compliant CellularRAM device (MT45W1MW16PD) with two SRAM devices with differing CE# interfaces:

- Single-CE#: Cypress 4Mb CY62147DV18
- Dual-CE#: Samsung 16Mb K6F1616R6C

## Power Supply Considerations

SRAM devices provide a number of power supply options, depending on manufacturer and customer requirements. The primary options are:

- Single 1.8V core power supply
- Single 3.0V core power supply
- Core power supply that does not equal the I/O voltage

The Micron CellularRAM device requires a 1.8V core supply with the option to run the I/O voltage at either 1.8V or 3.0V. This allows some flexibility in determining the transitional path for the design. An overview of these options are shown in Table 2.

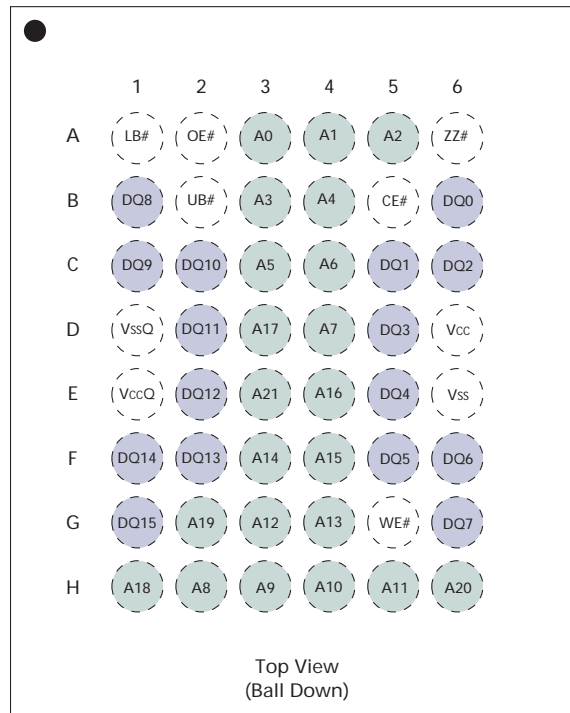
**Table 2: Power Supply Options**

SRAM Device Supply		Micron Device Supply		Notes
Core (Vcc)	I/O (Vcco)	Core (Vcc)	I/O (Vcco)	
1.65–1.95V	1.65–1.95V	1.70–1.95V	1.70–1.95V	1
2.7–3.3V	2.7–3.3V	1.70–1.95V	2.7–3.3V	2
2.7–3.3V	1.65–1.95V	1.70–1.95V	1.70–1.95V	2

- Notes:
1. No change to power supply connections.
  2. Reduce core voltage.

The supply differences noted in Table 2 require the system design to accommodate different supply voltages on the CellularRAM device VCC balls. See Figure 1 for the device ballout.

**Figure 1: Micron 48-Ball VFBGA Ballout Assignments**



SRAM devices provide the option to reduce the core supply to a lower data retention voltage without impacting the device's data storage ability. This reduced voltage is normally specified as 1.0V. For CellularRAM devices, VCC must not drop below VCC(MIN) to ensure correct operation of the device interface and data storage.

Both types of devices require an initialization period, once power is applied and stable, prior to the first access. For SRAM devices, the initialization period is  $t_{RC}$  (READ cycle time), whereas the CellularRAM device requires a longer period,  $t_{PU}$ . Although there is a timing difference—70ns ( $t_{RC}$ ) vs. 150 $\mu$ s ( $t_{PU}$ )—the inherent system delay until the first access makes this difference irrelevant.

## Memory Controller Interface

An SRAM memory controller interface can also control CellularRAM devices.

The basic control signals—WE#, OE#, and CE#—are the same for both the single- and dual-CE# SRAM and CellularRAM devices. However, the control signals—CE2 (dual-chip select SRAM) and ZZ# (CellularRAM device)—are different. These differences are listed in Table 3.

**Table 3: Control Signal (CE2/ZZ#) Differences**  
For more details, see “ZZ# Functionality” on page 6.

Device	Signal	Notes
Micron CellularRAM memory	ZZ#	Used to control PAR/DPD <sup>1</sup>
Dual-CE# SRAM	CE2	Used to control entry to data retention state
Single-CE# SRAM	NC	Low power achieved using supply voltage alone

Notes: 1. PAR/DPD can be also controlled via software access; see “Partial-Array Refresh/Deep Power-Down (PAR/DPD) Options” on page 7 for details.

Like SRAM, CellularRAM memory supports asynchronous READ and WRITE operations.

## Low-Power Settings

Both the SRAM and CellularRAM devices support options to reduce current consumption; however, different options are available per device (see Table 4).

**Table 4: Reduced-Current Options**

Device	Low-Power Current Mode	Enabled by
Single-CE# SRAM	Standby	CE# = HIGH with nominal Vcc
	Lower data retention	CE# = HIGH with data retention Vcc
Dual-CE# SRAM	Standby	CE1# and CE2 = HIGH CE2 = LOW with nominal Vcc
	Lower data retention	CE1# = HIGH with data retention Vcc
CellularRAM Memory <sup>1</sup>	PAR or DPD (ZZ# option)	CE# = HIGH; ZZ# = LOW with nominal Vcc
	PAR (software access option)	CE# and ZZ# = HIGH with nominal Vcc

Notes: 1. For more details, see “Partial-Array Refresh/Deep Power-Down (PAR/DPD) Options” on page 7.

## Low-Power Migration Options

SRAM's ability to enter a lower-power standby mode similar to that of CellularRAM memory varies by device:

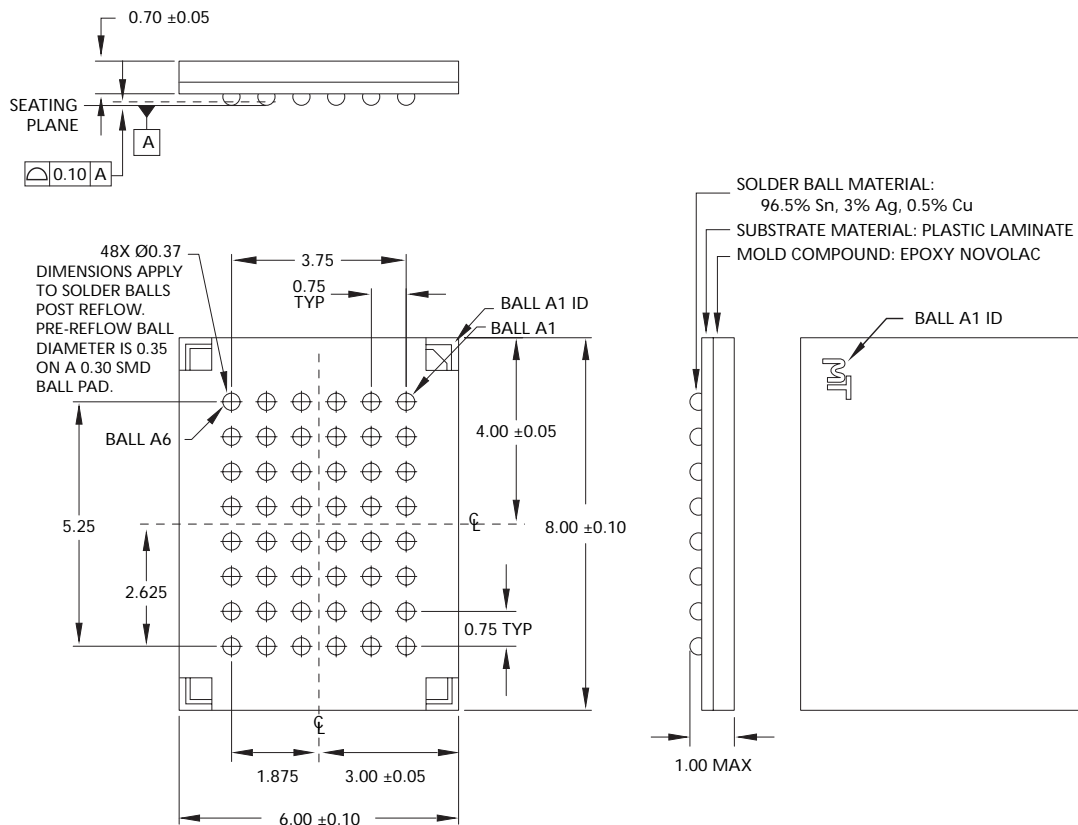
- Single-CE# SRAM lower-power standby currents require either:
  - Configuration register (CR) control via software access, or
  - The ability to control the ZZ# pin
- Dual-CE# SRAM lower-power standby currents require either:
  - CR control via software access, or
  - The ability to change the memory controller output that controls the CE2 pin

## Package Changes

Two package characteristics must be considered when making a PCB change to accommodate CellularRAM memory:

1. **Package size and type:** SRAM devices come in TSOP and 48-ball VFBGA packages. The Micron CellularRAM async/page device also uses a 48-ball, 0.75mm ball pitch VFBGA package.
2. **Ball/pin composition:** The market is moving to lead-free balls/pins, which will necessitate manufacturing process changes for some designs. See Figure 2 for CellularRAM package information.

**Figure 2: 48-ball VFBGA Package Drawing**



- Notes:
1. All dimensions in millimeters; MAX/MIN, or typical, as noted.
  2. Green packaging is available upon request.

## Added Benefits of Using CellularRAM Memory

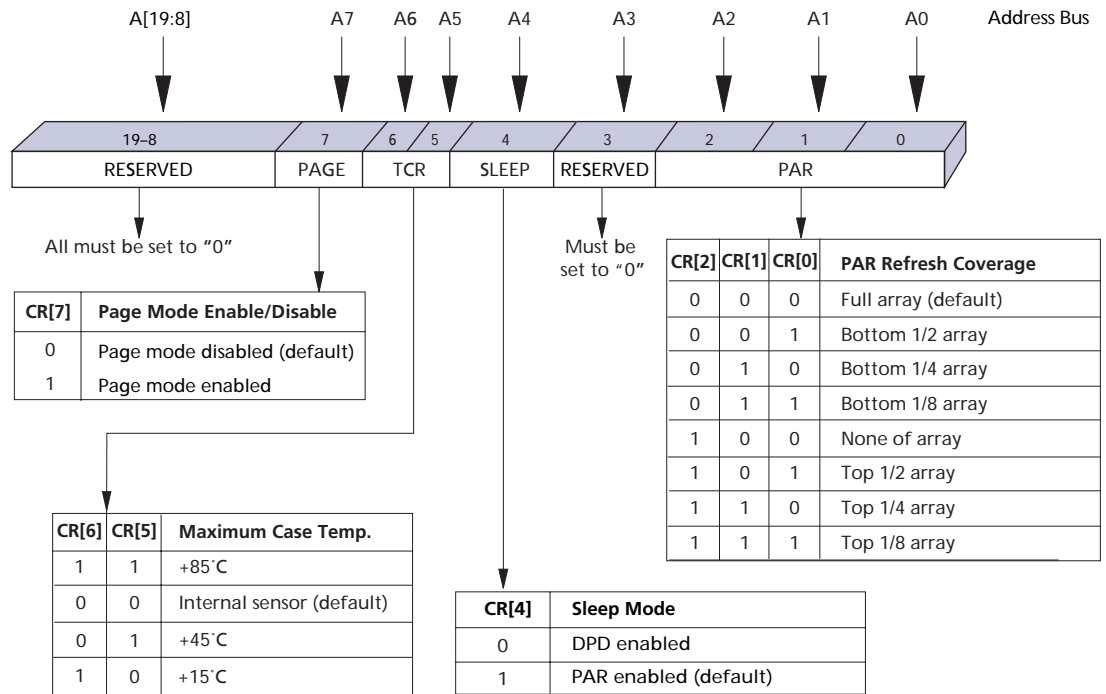
Replacing SRAM devices with CellularRAM devices typically requires a few easy changes, but any integration project should also consider what must be done to enable the design to take advantage of the additional features CellularRAM memory provides. See the following sections for details on enabling these features.

### Configuration Register (CR)

CellularRAM memory provides the added flexibility of configurable registers. The CR is accessible via either software- or hardware-initiated access. CR options available for the async/page CellularRAM device are shown in Figure 3.

The CR can configure PAR/DPD and enable page mode operation. For an overview of these functions, see subsequent sections of this technical note and the referenced Micron data sheet.

Figure 3: Configuration Register Bit Mapping



The CR can be set via either a software or hardware sequence and can be read using the software sequence. Both operations are described in the following two sections.

### ZZ# Functionality

The ZZ# pin works very much like the dual-CE# SRAM. If LOW for more than 10µs, ZZ# will enable the low-power options for the CellularRAM device. Once ZZ# returns HIGH, the CellularRAM device will be available immediately (PAR enabled) or after 150µs (DPD enabled).

ZZ# can also be used to modify the CR (see Figure 4). Reading the CR contents is only available via the software sequence.

**Software Access**

The CellularRAM specification defines a software sequence to allow configuration access to the CR. This sequence consists of four asynchronous operations—defined in Table 5—which allow the contents of the CR to be read or modified.

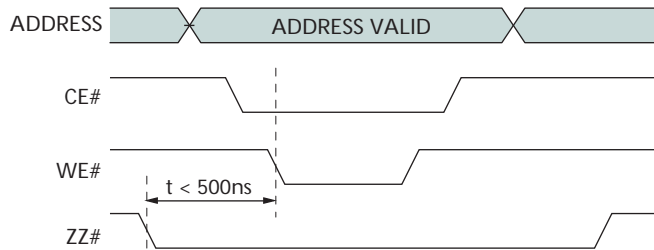
**Table 5: Software Access Configuration Sequence**

Cycle #	Operation	Address	Data
1	READ	MAX address	X
2	READ	MAX address	X
3	WRITE	MAX address	0x0000h
4	WRITE READ	MAX address MAX address	Configuration value in Configuration value out

Using the software sequence to modify the CR changes ZZ# default functionality until the next power cycle. Therefore, ZZ# can be pulled HIGH if DPD support is not required. PAR settings are set as soon as the WRITE to the CR is complete.

If the software sequence is used only to read the CR, then the ZZ# default functionality is not changed.

**Figure 4: Load Configuration Register Operation**



**Partial-Array Refresh/Deep Power-Down (PAR/DPD) Options**

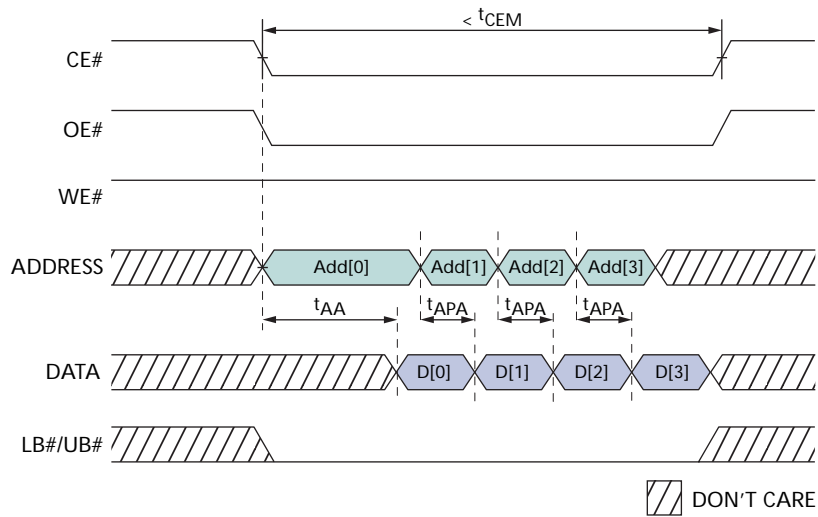
The CellularRAM device allows two different low-power configurations—PAR and DPD. The main difference between the two is that in PAR, array refresh occurs only in the selected portion of the array, while refresh is disabled for the entire array during DPD.

Once the PAR/DPD operation is completed, full array refresh is enabled and normal device operation will occur immediately (PAR enabled) or after 150µs (DPD enabled).

**Page Mode**

The CellularRAM device allows the memory controller/device interface to operate at a speed higher than typical asynchronous speeds. This operation is a performance-enhancing extension of legacy asynchronous READ operation. Figure 5 on page 8 shows the timing changes associated when comparing interpage and intrapage operations.

Figure 5: Page Mode READ Operation



## Other CellularRAM Devices

Micron's 16Mb CellularRAM device (MT45W1MW16PD) is the async/page version of the CR1.0 specification. Also contained within the 1.0 specification is support for an async/page/burst, 54-ball VFBGA device, which can also be configured to operate in async/page mode only.

Other CellularRAM devices in the family support both higher frequencies and extended functionality, which provides options for increased density, functionality, and speed. Further details on the CellularRAM product family are available on Micron's Web site: [www.micron.com/products/psram](http://www.micron.com/products/psram).

## Conclusion

The changes required to convert a design from a single- or dual-chip select (CE#) SRAM device to Micron CellularRAM memory are easily accomplished and provide several benefits. Design considerations include power supply differences, changes to the memory controller interface, low-power settings, and package changes.

The benefits of switching from SRAM to CellularRAM memory include:

- Compatibility to previous-generation SRAM and future-generation burst NOR Flash memory
- Software access to the configuration register
- Multiple vendors (via the standardized specification)
- High-speed interface with several low-power modes

For further technical assistance, e-mail [psramsupport@micron.com](mailto:psramsupport@micron.com) or visit Micron's Web site: [www.micron.com/products/psram](http://www.micron.com/products/psram).

## References

- Micron CellularRAM data sheet—MT45W1MW16PD  
[www.micron.com/products/psram](http://www.micron.com/products/psram)



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