Technical Note

Low-Power Options for Async/Page CellularRAM™

Introduction

Micron® CellularRAM™ devices are designed to be backward compatible with 6T SRAM, early-generation asynchronous, and page PSRAM. This backward compatibility is essential for designs requiring high-speed and low-power operation. CellularRAM memory also provides a burst NOR Flash-compatible interface that allows designers to take their designs to the next performance level.

CellularRAM device features include:

- Support for 16Mb through 128Mb densities
- Small-package footprint FBGA devices
- Known good devices (KGD)
- Burst NOR Flash compatible interface
- Asynchronous, page, and high-speed (up to 104 MHz) burst interface
- Low-power options, including partial array refresh (PAR), low standby current, and deep power-down (DPD) mode
- Hidden refresh control

This technical note describes the low-power operational modes available on the asynchronous/page CellularRAM devices and the use of the ZZ# input in conjunction with the configuration register (CR) settings to control these modes.

This document is separated into the following sections:

1. Low-power operation modes
2. Configuring the device

This document applies specifically to the 48-ball async/page 16Mb, CR1.0-compliant device, the MT45W1MW16PD. However, the concepts covered in this technical note apply to other Micron PSRAM/CellularRAM devices.

Low-Power Operation Modes

Async/page CellularRAM devices are designed with multiple options to reduce the current consumption of the device. System designers are able to utilize these options by using a combination of the CR settings and the ZZ# pin functionality.

The low-power modes available are temperature compensated refresh (TCR), standby mode, partial array refresh (PAR), and deep power-down (DPD). Table 1 shows the overview of control signal states and CR settings required to support these modes.

Table 1: Low Power Operational Modes

Operational Mode	Control Signals		Configuration Register Settings		
	CE#	ZZ#	CR[6:5]	CR[4]	CR[2:0]
TCR	X	X	00h[1]	1	N/A
Standby	H	H	00h[1]	1	N/A
PAR	H	L	00h[1]	1	Refresh coverage
DPD	H	L	N/A	0	N/A

Notes: 1. Refer to the section below for further details.

Temperature Compensated Refresh

Temperature compensated refresh (TCR) is controlled by CR[6:5] and can be used by the designer to select the appropriate setting of the internal refresh oscillator frequency. This is critical for the DRAM cell, which is the basis of the CellularRAM device, since cell leakage will change with device temperature. An increase in temperature will result in a higher leakage current, while a lowering in the device temperature will result in a reduction in leakage current.

Given this, TCR is the first option available to the designer since this will set the required "maximum device temperature" for the internal refresh oscillator setting. Optimum operation is achieved by enabling the internal sensor (CR[6:5] = 00h), since this allows the refresh rate to be automatically adjusted, depending on the operating temperature. The available options are detailed in Table 2.

Table 2: Temperature Compensated Refresh (CR[6:5])

TCR Mode	CR[6]	CR[5]
+85°C	1	1
Internal sensor (default)	0	0
+45°C	0	1
+15°C	0	0

Note: The recommended mode is to enable the internal sensor (CR[6:5] = 00h).

Standby

When deselected, CE# = HIGH, the CellularRAM device enters standby mode. In this mode, the TCR setting will determine the rate for full-array refresh (PAR is not enabled unless ZZ# = LOW).

Partial Array Refresh (PAR)

The PAR bits restrict REFRESH operation to a portion of the total memory array when the sleep mode is set to PAR (CR[4] = 1) and when a PAR-enabled refresh occurs. This feature allows the system to reduce current by only refreshing the part of the memory array required by the application; see Table 3 for coverage details.

Table 3: PAR Refresh Coverage (CR[2:0])

PAR Refresh Coverage	CR[2]	CR[1]	CR[0]
Full-array (default)	0	0	0
Bottom 1/2 array	0	0	1
Bottom 1/4 array	0	1	0
Bottom 1/8 array	0	1	1
None of array	1	0	0
Top 1/2 array	1	0	1
Top 1/4 array	1	1	0
Top 1/8 array	1	1	1

The enabling of PAR can be accomplished by using either software or hardware control.

To re-enable the full-array refresh, the memory controller performs one of the following operations:

- If ZZ# is used to modify the CR settings, then full-array refresh will start when ZZ# is de-asserted.
- If software access is used to modify the CR settings, then PAR will need to be set, via software access, to full-array refresh (CR[2:0] = 0x000b).

Deep Power-down (DPD)

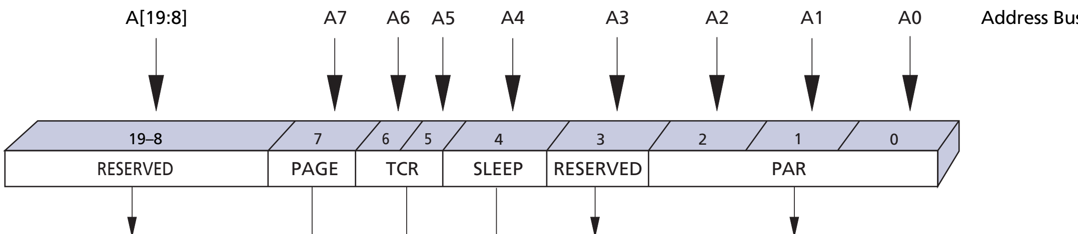
DPD operation disables all refresh-related activity. This mode is used when the system does not require data storage provided by the CellularRAM device. Any stored data becomes corrupted when DPD is enabled.

DPD is enabled by setting sleep mode to DPD (CR[4] = 0), and then asserting ZZ# for longer than 10µs. When returning the CellularRAM device to normal operation, de-asserting ZZ# causes the device to begin a 150µs initialization period. Once the initialization period is complete, the device will be in the refresh state defined by the CR. DPD operation cannot be enabled by the software access mode.

Configuring the Device

Using hardware or software control, the memory controller configures the CR to control the operational mode of the async/page CellularRAM device. The CR controls the page mode operation, PAR refresh coverage, DPD enabling, and TCR control; see Figure 1 below.

Figure 1: Configuration Register Bit Mapping



CR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enabled

CR[6]	CR[5]	Maximum Case Temp.
1	1	+85°C
0	0	Internal sensor (default)
0	1	+45°C
1	0	+15°C

CR[4]	Sleep Mode
0	DPD Enabled
1	PAR Enabled (default)

CR[2]	CR[1]	CR[0]	PAR Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

Software Operation

For systems that cannot control the ZZ# input, the contents of the CR can be read or modified using a software sequence.

As detailed in Table 4, the CR software access consists of a four-step sequence to the maximum memory address for the device. The contents of this address is not changed by using this sequence.

Table 4: Software-Controlled Configuration Sequence

Cycle #	Operation	Address A[19:0]	Data DQ[15:0]
1	READ	MAX Address	X
2	READ	MAX Address	X
3	WRITE	MAX Address	Register select
4	WRITE READ	MAX Address MAX Address	Configuration value in Configuration value out

Once a successful load of the CR is performed using the software access sequence, the functionality of the ZZ# input will be modified. This modification in ZZ# functionality remains until the next time the device is powered-up; see "Hardware Operation (ZZ#)" on page 6 for more details. If the software operation is only used to READ the contents of the CR, then the functionality of the ZZ# input is not affected.

Figures 2 and 3 show the CR load and READ operations.

Figure 2: Software Access Load Configuration Register

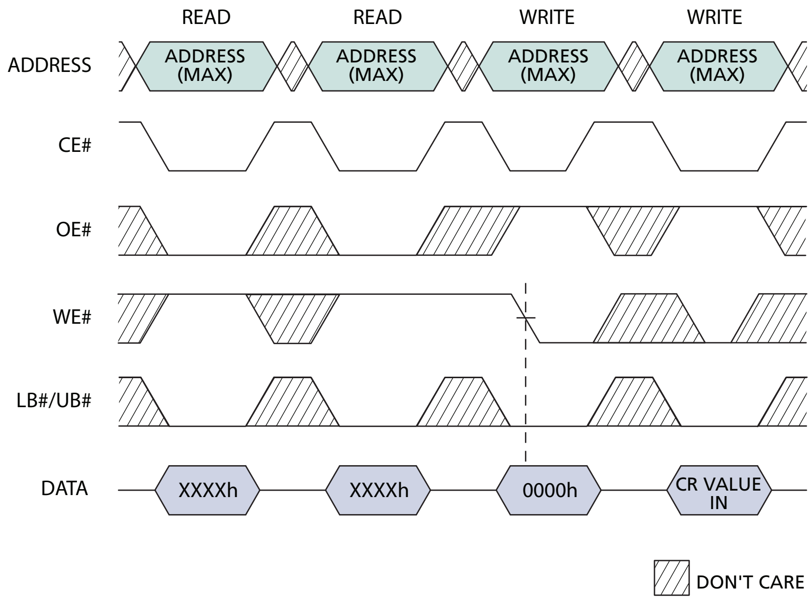
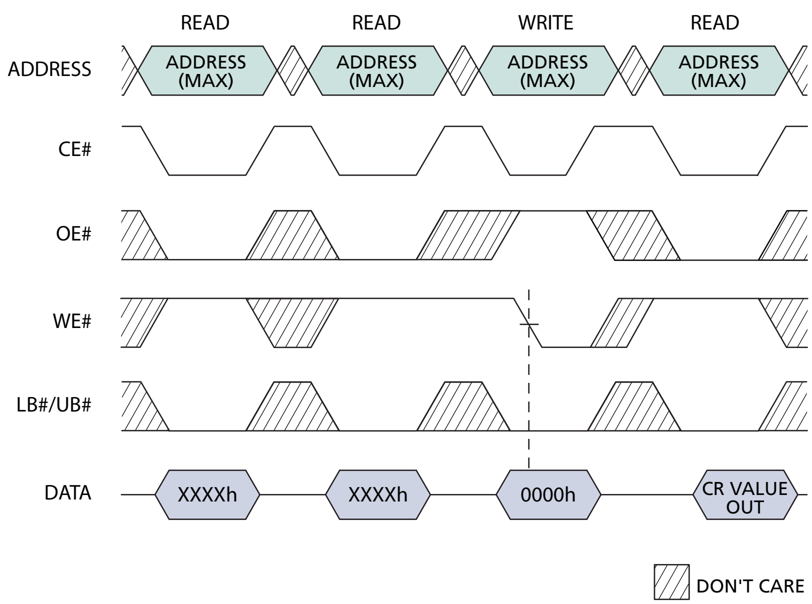


Figure 3: Software Access Read Configuration Register



Hardware Operation (ZZ#)

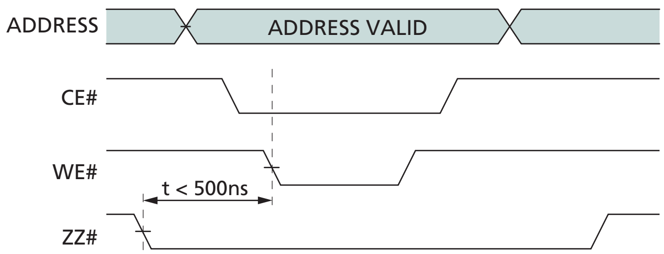
The CellularRAM device ZZ# input performs two functions:

1. modifying the CR
2. enabling the selected sleep mode

Modifying the CR

The contents of the CR can be modified by asserting ZZ# and then issuing a WRITE operation (see Figure 4). The value placed on the address bus (A[19:0]) will be latched into the CR on the rising edge of CE# or WE#, whichever occurs first. The CR cannot be read using the ZZ# input.

Figure 4: Load Configuration Register Operation



Enabling Sleep Mode

The ZZ# input can be used to enable sleep mode (PAR or DPD) with the understanding that if software access mode is used to modify the CR, then ZZ# can only be used to enable DPD. Then, PAR can only be enabled via software access to the CR. Once ZZ# is de-asserted, sleep mode will be disabled and normal operation can be resumed instantaneously (sleep mode = PAR) or within 150µs (sleep mode = DPD).

Controlling ZZ#

The ZZ# input can be controlled one of two ways:

1. If the ZZ# input is not required, it can be tied directly to $V_{CC}Q$.
2. If the ZZ# input is required to control the low-power functionality, then a GPIO output from the memory controller will be required.

Conclusion

This technical note discussed the low-power options available on the async/page CellularRAM devices.

The primary points are:

- Understanding and utilizing the multiple, low-power modes
- Configuring the devices
- Controlling ZZ# input

For further technical assistance, e-mail psramsupport@micron.com or visit Micron's Web site: www.micron.com/products/psram.

References

- Micron CellularRAM data sheet—MT45W1MW16PD at www.micron.com/products/psram/cellularram

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992