

Technical Note

Variable vs. Fixed Latency CellularRAM™ Operation

Introduction

Micron® CellularRAM™ devices are designed to be backward compatible with 6T SRAM and early-generation asynchronous/page PSRAM. Backward compatibility is essential for designs requiring high speed and low-power operation. CellularRAM memory also provides an interface that is compatible with burst NOR Flash. This interface allows designers to take their designs to the next performance level.

CellularRAM device features include:

- 16Mb through 128Mb density support
- Small-package footprint FBGA devices
- Known good die (KGD)
- Burst NOR Flash compatible interface
- Asynchronous, page, and high-speed (up to 133MHz) burst interface
- Low-power options: partial array refresh (PAR), low standby current, deep power-down (DPD) mode
- Hidden refresh control

This technical note describes the differences between variable and fixed latency burst mode operation and the impact that this has on the memory controller/CellularRAM interface. This document is separated into the following sections:

- Variable latency mode operation
- Fixed latency mode operation
- WAIT pin operation

The detailed device information specifically applies to the 54-ball asynchronous/page/burst 64Mb, CR1.5-compliant device (MT45W4MW16BC). However, the concepts presented in this technical note apply to other Micron burst mode CellularRAM devices.

Burst Mode Overview

CellularRAM devices are designed to work seamlessly on a burst Flash NOR bus. CellularRAM devices are configured via the bus configuration register (BCR) to work with the required memory controller interface. The CellularRAM device will be configured for burst operation when BCR[15] = 1.

To achieve maximum throughput, data must be provided at the required point within the burst cycle. Providing data at the required point is the key to a optimal memory controller/device interface. Micron CellularRAM devices support variable and fixed latency modes that can be configured by a combination of BCR[14] and BCR[13:11]. The following sections will describe these two operational modes in detail.

Variable Latency Mode

Variable latency configures the CellularRAM device for minimum latency at the highest clock frequencies supported by the device. In this mode, the memory controller needs to monitor WAIT to detect any conflict when a refresh request occurs at the start of the burst operation. In variable latency mode, the number of clock cycles before the first data transfer will differ depending on whether there is a refresh request pending. Table 1 shows the permitted latency configuration codes for the 64Mb CR1.5 CellularRAM device. Note that other CellularRAM devices may support latency configuration codes.

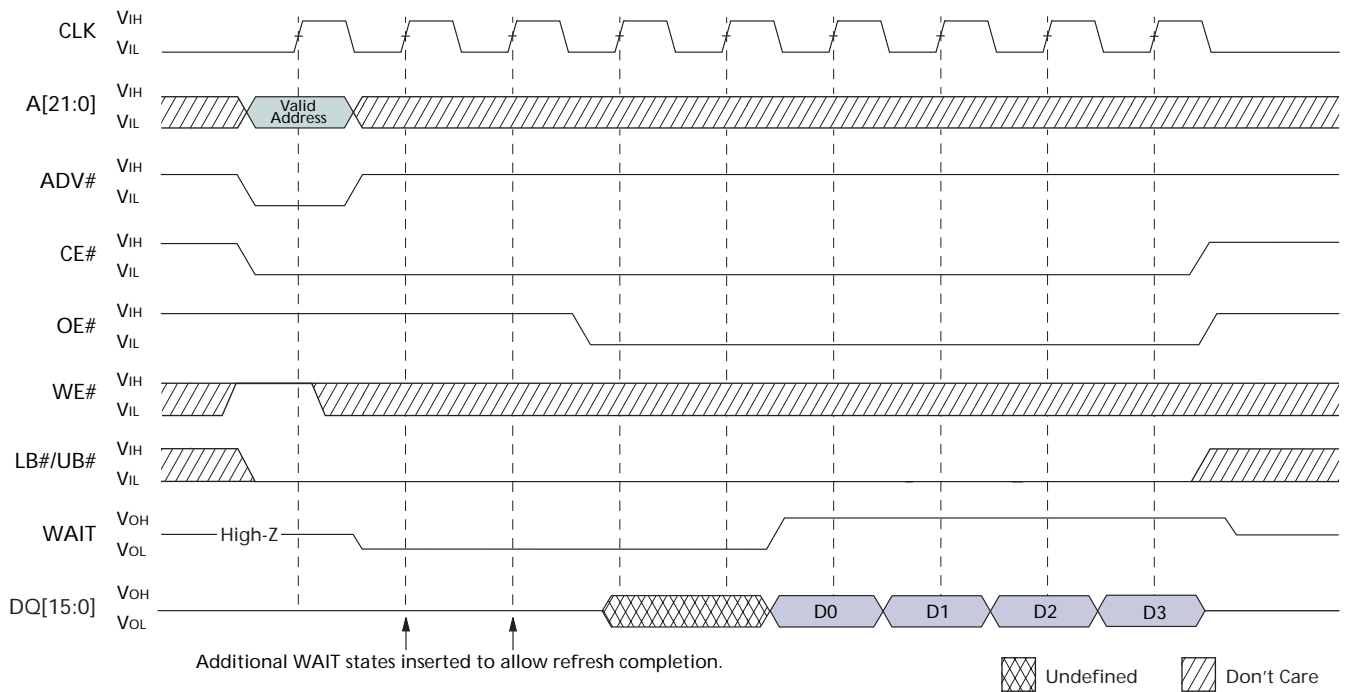
Table 1: Variable Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency		Max Input CLK Frequency (MHz)	
		Normal	Refresh Collision	104 MHz	80 MHz
010	2 (3 clocks)	2	4	66 (15ns)	52 (19.2ns)
011	3 (4 clocks)—default	3	6	104 (9.62ns)	80 (12.5ns)
Others	Reserved	–	–	–	–

Note: Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.

The number of instances where a “push out” occurs on the initial burst latency depends heavily on the usage of the device. An example of the impact on the timing of the initial access is shown in Figure 1 on page 3.

Figure 1: Refresh Collision during Variable Latency READ Operation



Note: Non-default BCR settings for refresh collision during variable latency READ operation: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.

Fixed Latency Mode

Fixed latency configures the CellularRAM device to account for the worse-case access delay due to a refresh request. This latency will occur for all initial Burst accesses. In this mode, the first access is now deterministic and the memory controller design determines whether the memory controller monitors the WAIT signal.

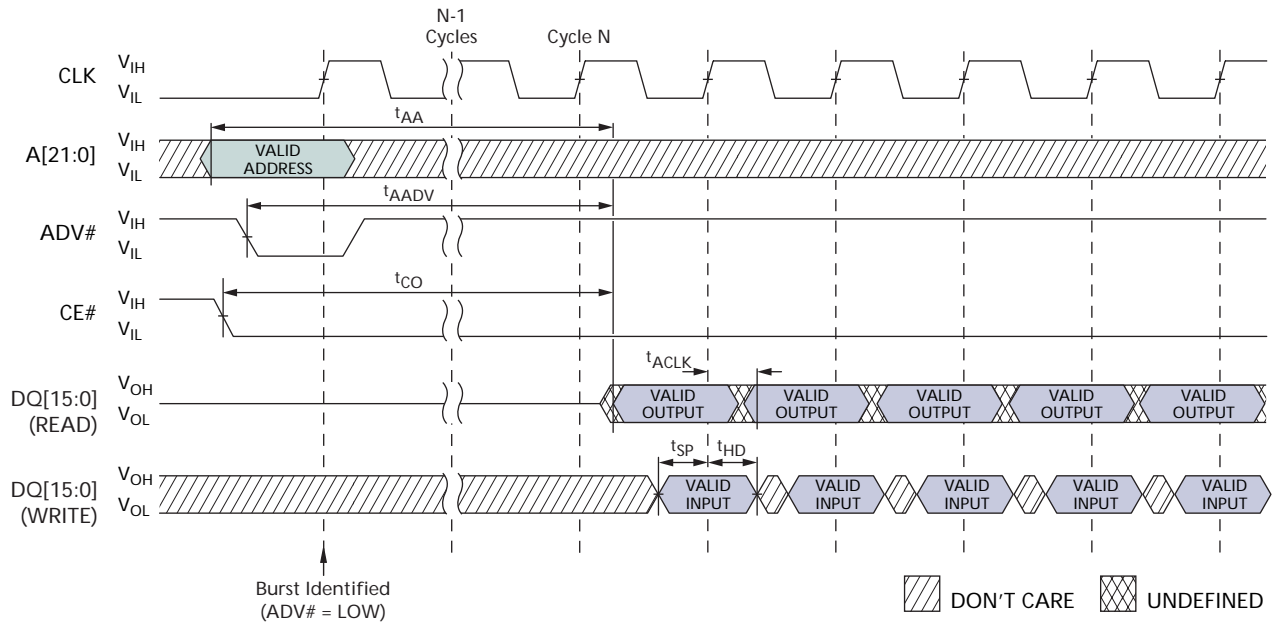
Table 2 shows the permitted fixed latency configuration codes for the 64Mb CR1.5 CellularRAM device.

Table 2: Fixed Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency Count (N)	Max Input CLK Frequency (MHz)	
			104 MHz	80 MHz
010	2 (3 clocks)	2	33 (30ns)	33 (30ns)
011	3 (4 clocks)—default	3	52 (19.2ns)	52 (19.2ns)
100	4 (5 clocks)	4	66 (15ns)	66 (15ns)
101	5 (6 clocks)	5	75 (13.3ns)	75 (13.3ns)
110	6 (7 clocks)	6	104 (9.62ns)	80 (12.5ns)
Others	Reserved	—	—	—

All timing diagrams for a fixed latency show a deterministic first burst access, as shown in Figure 2 on page 4.

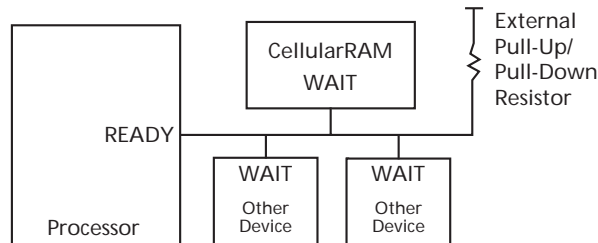
Figure 2: Fixed Latency READ Operation



WAIT Pin Operation

The WAIT output, as mentioned previously, is key to the burst memory controller/CellularRAM interface and is typically connected to the shared system level WAIT signal (see Figure 3). The WAIT output is asserted at the start of the cycle, the active level being defined by BCR[10], and then WAIT is de-asserted prior to the first data cycle, depending on the WAIT configuration (BCR[8]). Once the device is deselected, the CellularRAM device WAIT output will return to High-Z to allow another device to be able to control the memory controller WAIT input.

Figure 3: Wired-OR WAIT Configuration



For fixed latency burst operation, the WAIT pin can be ignored if the memory controller can handle the deterministic accesses without the need for the WAIT input, or can be connected (as shown in Figure 3) if the memory controller requires this input.

Fixed Latency Support for Micron CellularRAM Devices

Micron CellularRAM devices offer many types of support for variable and fixed latency operation during burst operations. Table 3 shows the support per device.

Table 3: Latency Support per Density

Density	Part Number	Latency Supported		Notes
		Variable	Fixed	
16Mb	MT45W1MW16BA	Yes	No	
16Mb	MT45W1MW16BD	Yes	Yes	1
32Mb	MT45W2MW16BA	Yes	No	
64Mb	MT45W4MW16B	Yes	Yes	1
64Mb	MT45W4MW16BC	Yes	Yes	2
128Mb	MT45W8MW16B	Yes	Yes	2

Notes: 1. Fixed latency support is outside of the CellularRAM Working Group (CRWG) CR1.0 definition. For details on fixed latency code support, please contact Micron.
 2. Fixed latency code support is CRWG CR1.5 compliant.

Conclusion

Several burst mode latency options are available on the async/page/burst CellularRAM devices and designers need to be aware of how the choice of latency options will impact their designs.

The main considerations described in this tech note are:

- Understanding the differences between variable and fixed latency operation
- Differences in the deterministic nature of the first data access
- Control of the WAIT output

By understanding the implications of the options, the designer can obtain maximum performance from the target system.

For further technical assistance, e-mail psramsupport@micron.com or visit Micron's Web site: <http://www.micron.com/products/psram>.

References

Micron CellularRAM data sheet—MT45W4MW16BC
 (<http://www.micron.com/products/psram/cellularram>)



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