

Technical Note

Designing with CellularRAM™ Memory on a NOR Flash Bus

Introduction

Micron® CellularRAM™ devices are designed to be backward compatible with 6T SRAM, early-generation asynchronous, and page PSRAM. But they also offer a burst NOR Flash compatible interface, which allows natural expansion of the NOR interface to support a volatile memory device, enabling increased design performance.

NOR Flash devices are key system components because they are the primary storage device for operation and application code. Historically, however, the total system usage of the NOR Flash interface has not been high once the initial system code load is completed.

This technical note describes how to design CellularRAM memory on a NOR Flash bus. Specifically, it addresses the following areas:

- CellularRAM Memory/NOR Flash overview and comparison
- Interface overview
- CellularRAM device configuration
- Memory map considerations and connectivity diagrams

Table 1 provides an overview of comparative device features.

Table 1: Comparative Device Features: CellularRAM Memory vs. NOR Flash

Function		CellularRAM Memory	NOR Flash	Notes
Power supply	Core	1.70–1.95V	1.70–1.95V/3.30V	1
	I/O	1.70–1.95V/3.30V	1.70–1.95V/3.30V	1
Bus interface support	Async (READ/WRITE)	Yes	Yes	
	Page READ	Yes	Yes	
	Burst READ	Yes	Yes	
	Burst WRITE	Yes	No	
Address scheme		Broadside	Broadside	
Registers	Burst interface	Bus configuration register (BCR) Refresh configuration register (RCR) Device identification register (DIDR)	Read configuration register (RCR) Enhanced configuration register (ECR)	
	Async/page Interface	Configuration register (CR)	-	
Mixed mode operation		Supported	Supported	
Low-power options		Standby Deep power-down (DPD) Temperature-compensated refresh (TCR)	Standby Deep power-down (DPD)	
Cell architecture		Volatile DRAM cell	Non-volatile Flash cell	

Notes: 1. Maximum voltage is device dependent

Device Overview

NOR Flash

A number of memory suppliers provide NOR-based Flash devices, enabling designers to choose from a variety of configurations. NOR Flash devices evolved from a pure asynchronous READ/WRITE interface, to page mode READ, then to burst mode READ operation.

CellularRAM Memory

CellularRAM memory is based on DRAM technology and supports a high-speed memory interface, while meeting the additional requirement for low-power operating modes. The CellularRAM Workgroup common specification allows a designer to consider multiple sourcing.

Micron CellularRAM memory is targeted at NOR Flash applications where it can provide additional functionality for the NOR Flash interface.

CellularRAM device features include:

- Support for 16Mb through 256Mb densities
- Small-package footprint FBGA devices
- Known good die (KGD)
- Burst NOR Flash compatible interface
- Asynchronous, page, and high-speed (up to 133 MHz) burst interface
- Low-power options including partial array refresh (PAR), low standby current, and deep power-down (DPD) mode
- Hidden refresh control

This technical note focuses on both the async/page/burst 128Mb, CR1.5-compliant MT45W8MW16B and the async/page 16Mb, CR1.0-compliant MT45W1MW16PD devices.

Asynchronous READ/WRITE Access

Overview

A NOR Flash asynchronous READ/WRITE access is the most basic device operation. For every access, a valid address must be provided to access that memory location.

CellularRAM Memory

The CellularRAM device supports a standard NOR Flash asynchronous operation (see Figures 1 and 2). The CellularRAM device also supports address transition detection (ATD) that allows CE# to remain asserted (LOW) between consecutive accesses. The address change initiates a new async operation. With any async WRITE operation, a designer must ensure that $t_{CEM}^{(MAX)}$ is not violated. For further detail, see “CellularRAM Hidden Refresh” on page 11.

Figure 1: READ Cycle

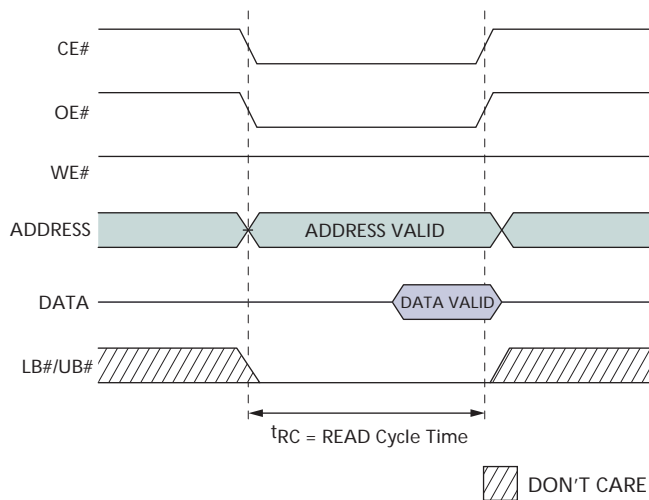
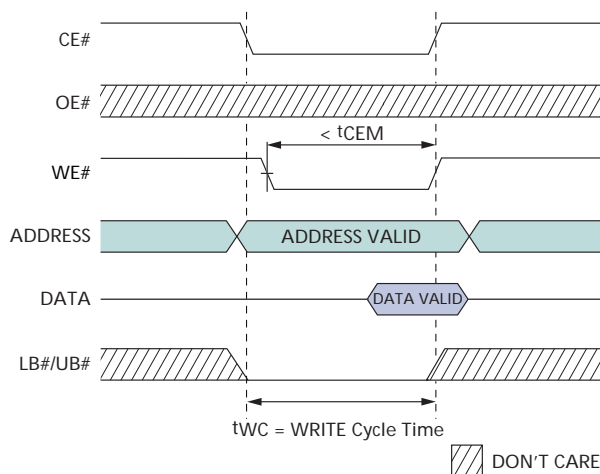


Figure 2: WRITE Cycle



Page Mode READ Access

Overview

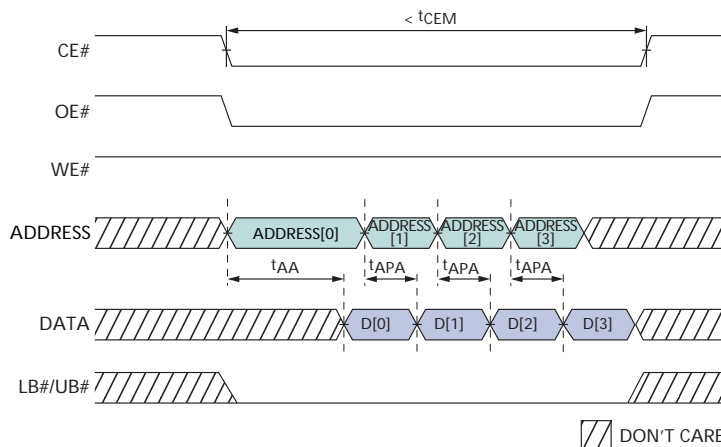
NOR Flash page mode READ operations are an enhancement over async READ operations and utilize an internal device buffer to access memory locations within a page of memory. This page size can range from 4 to 32 words.

A page mode READ operation is divided into two sections, (1) the initial interpage access and (2) the subsequent intrapage accesses. The interpage address, when supplied to the device, results in a data access time for this cycle at the standard async operation timing (t_{AA}) and the loading of the data from subsequent page addresses into internal registers. With the internal registers loaded, any subsequent access at an address that lies within the page boundary results in the internal registers being accessed. Thus leading to an intrapage access (t_{APA}). (Note that t_{APA} is much less than t_{AA} .)

CellularRAM Memory

CellularRAM memory supports a standard 16-word NOR Flash page mode READ operation (see Figure 3), but the designer must configure the device's refresh configuration register (RCR) to operate in page mode (RCR[7] = 1). For page mode READ operations, $t_{CEM}^{(MAX)}$ must not be violated (see "CellularRAM Hidden Refresh" on page 11).

Figure 3: Page Mode READ



Burst Access

Overview

NOR Flash synchronous burst mode READ access was introduced to improve the speed of the interface between the NOR Flash device and the memory controller. This change allows more system code execution directly from the device. To allow for this new synchronous operation, both the memory controller and memory device added the CLK, ADV#, and WAIT signals as well as a configuration register. Currently, speeds up to 133 MHz are supported on the NOR Flash interface.

A burst operation consists of a multiclock sequence that must be performed in an ordered fashion to ensure the correct operation of the interface. The main difference between burst and page mode operation is that the memory controller only supplies the initial address. All subsequent addresses are incremented internally by the memory device to continue the burst operation.

The result of this configuration is that memory accesses will continue on subsequent rising memory clock edges, after an initial latency, until a new address is supplied, or the device is deselected (CE# = HIGH).

CellularRAM Memory

CellularRAM devices support both the standard NOR Flash burst READ (see Figure 4) and the additional burst WRITE operation (see Figure 5 on page 6). $t_{CEM}(\text{MAX})$ must not be violated (see “CellularRAM Hidden Refresh” on page 11).

To configure the CellularRAM device to support burst operation, the bus configuration register BCR[15] must be set to “1.” Other options must be configured via the BCR to ensure that the interface between the memory controller and the CellularRAM device is working correctly.

Figure 4: Burst READ

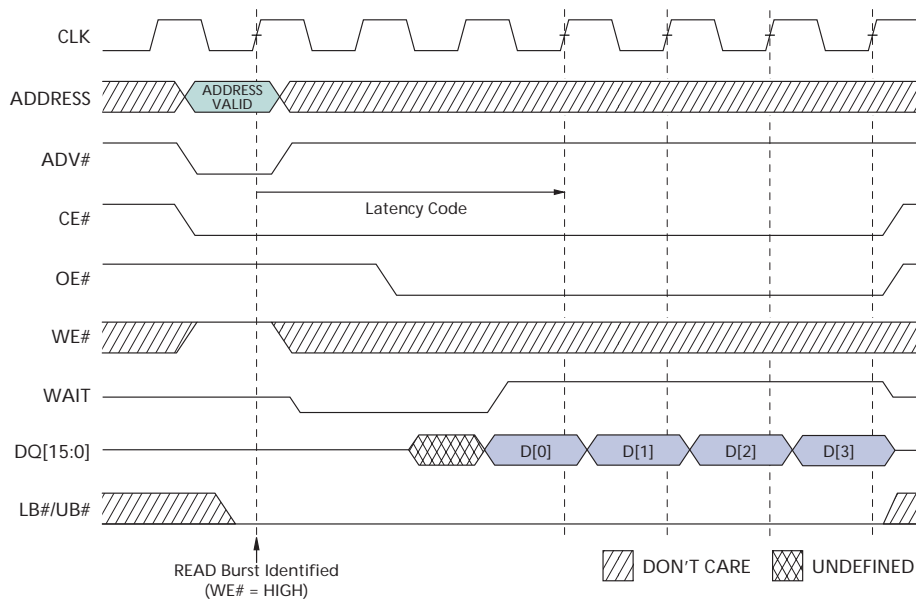
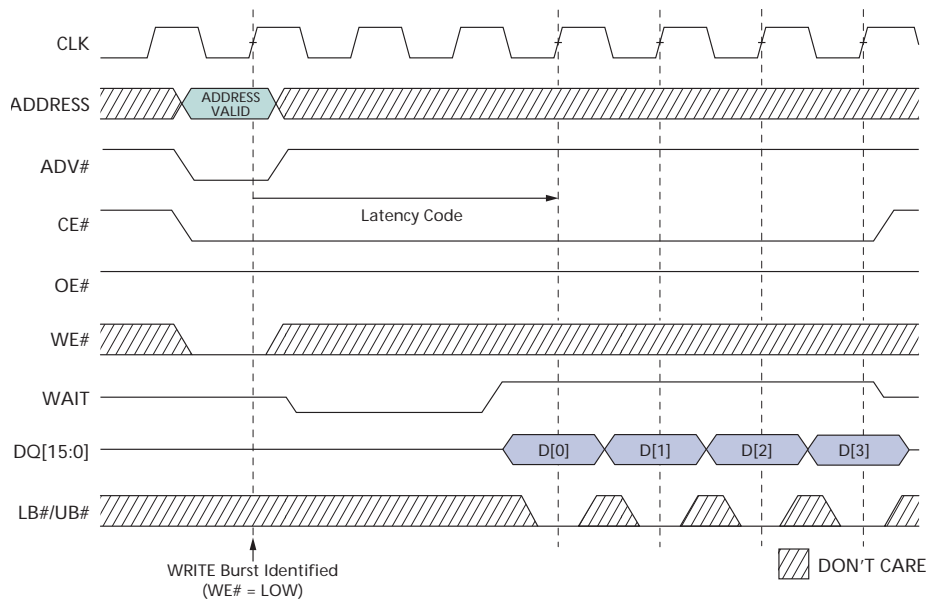


Figure 5: Burst WRITE



Mixed Mode Operation

Overview

Mixed mode operation is defined as the ability of a device to work seamlessly when making a transition from consecutive async to burst or burst to async operations. This is beneficial when attempting to maximize system bandwidth for the burst READ mode, while still allowing access of a device asynchronously for memory WRITES or device configuration requirements.

CellularRAM Memory

The CellularRAM device can implement mixed mode operation by (1) changing the device configuration or (2) stopping the CLK. The memory controller and system design dictate which method is best.

Using BCR[15]

The operating mode BCR[15] bit controls whether the device will function in synchronous burst access mode (BCR[15] = 0) or in asynchronous access mode (BCR[15] = 1). The memory controller can change the value for BCR[15] to switch between the two operational modes, if required. One benefit of using this mode change method is that the CLK input can remain active for both modes.

Stopping the CLK Signal

Memory controllers that stop the CLK signal for asynchronous operations allow the CellularRAM device to remain configured for synchronous burst access mode (BCR[15] = 0), enabling a simpler method for switching between modes. Examples of this mode switch are shown in Figure 6 and Figure 7 on page 7.

Note: For both mixed mode operations, the ADV# input can either be used to “latch” the address during async operation, or left LOW during the whole async operation.

Device Configuration

Several registers are used to configure the CellularRAM memory controller interface. The registers available on CR1.5-compliant burst CellularRAM devices are:

- Bus configuration register (BCR)
- Refresh configuration register (RCR)
- Device identification register (DIDR)

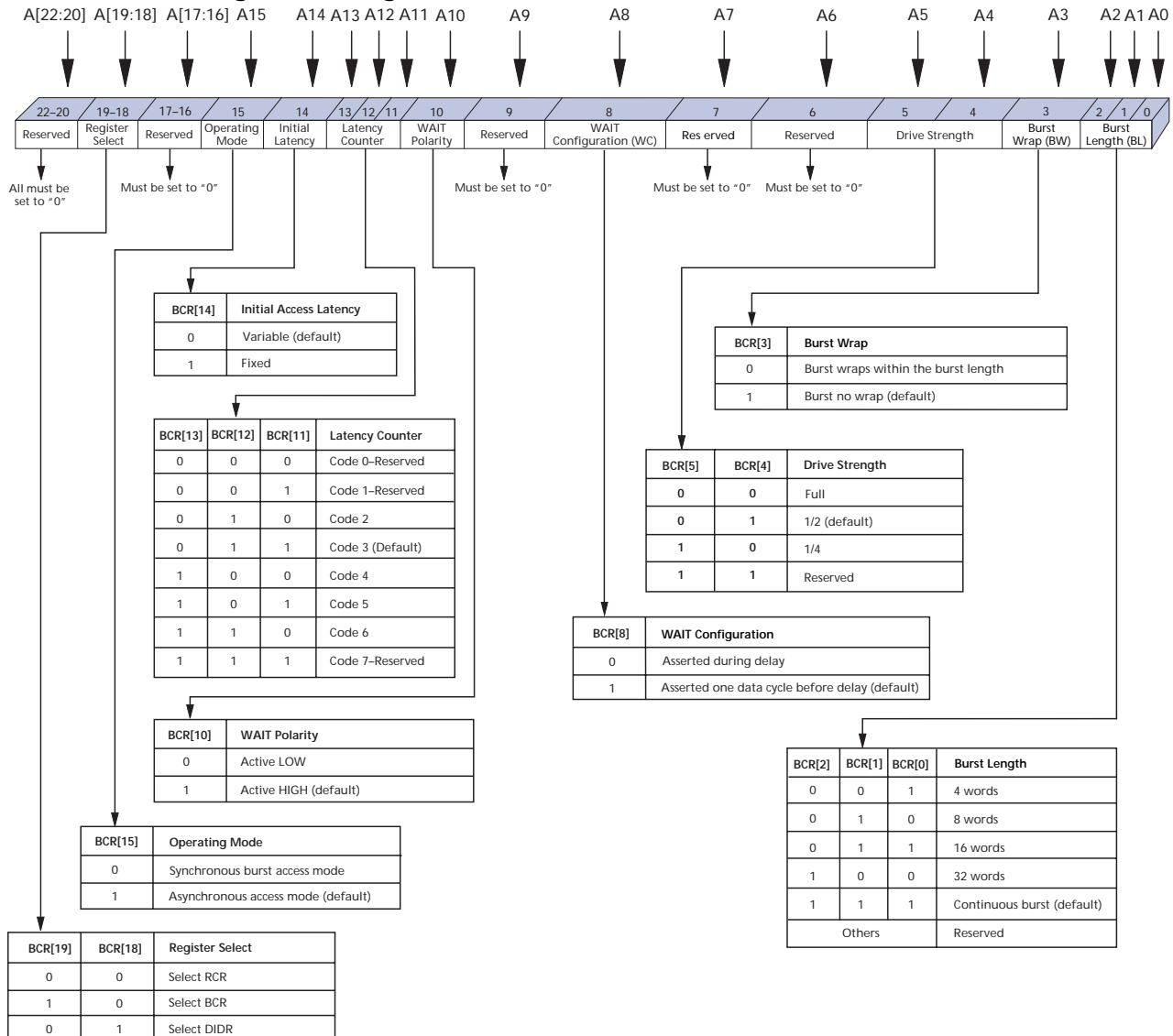
The async/page CellularRAM device has one register, the configuration register (CR).

The following sections provide an overview of each register and how the registers can be accessed by the memory controller.

Bus Configuration Register (BCR)

The BCR is used on burst-capable CellularRAM memory to control the operating mode of the device. Figure 8 shows the BCR options available.

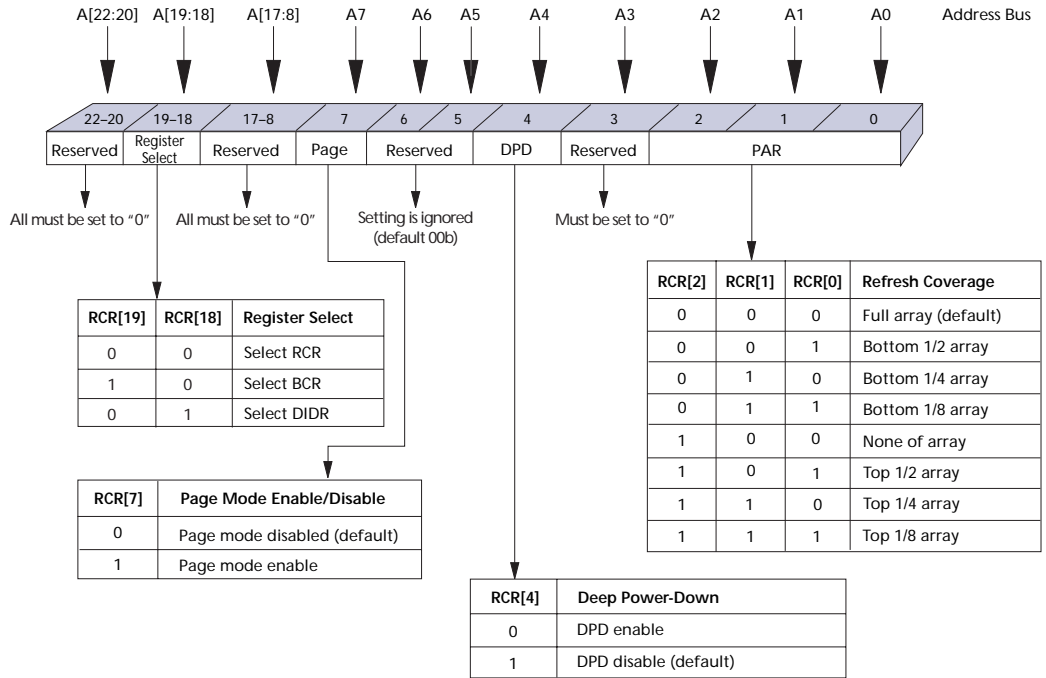
Figure 8: Bus Configuration Register



Refresh Configuration Register (RCR)

The RCR is used on burst-capable CellularRAM devices to control the transparent self-refresh capabilities of the device. Changing the values contained within the RCR can dramatically reduce the refresh current during standby modes. The RCR is also used to control whether the device is enabled for page READ mode. Figure 9 shows the RCR options available.

Figure 9: Refresh Configuration Register



Async/page CellularRAM devices have one CR. The options available are the same as those shown for the RCR in Figure 9.

Device Identification Register (DIDR)

The introduction of NOR Flash devices prompted a system requirement for a way to identify which Flash device was present without visually checking the device. This identification process was specified in the JEDEC Common Flash Interface (CFI) specification. The CellularRAM specification includes a simplified form—the DIDR—on CR1.5-compliant and later devices. Table 2 shows available DIDR options.

Table 2: Device Identification Register Mapping

Bit Field	DIDR[15]	DIDR[14:11]		DIDR[10:8]	DIDR[7:5]	DIDR[4:0]
Field name	Row length	Device version		Device density	CellularRAM generation	Vendor ID
		Bit setting	Version			
Bit setting	0b	0000b	1st	011b	010b	00011b
		0001b	2nd			
Meaning	128 words			128Mb	CellularRAM 1.5	Micron

Notes: 1. Vendors with 256-word row lengths for CellularRAM 1.5 devices will set DIDR[15] to 1b.

Register Access

Access to CellularRAM registers is supported by either a software or hardware-initiated method of control.

Software Access

CellularRAM registers can be accessed via a sequence of consecutive READ/WRITE operations to the maximum CellularRAM device address. For detailed information on how the software access mode works, see the “Software Access” section of the referenced burst CellularRAM device data sheet.

Hardware Access

The hardware access mode differs between burst and async/page CellularRAM devices.

- For the burst device, the CRE pin must be controlled by the memory controller.
- For the async/page device, the ZZ# pin must be controlled by the memory controller.

Full descriptions of these methods are included in the device data sheets.

Other Interface Considerations

Variable and Fixed Latency

The value contained within BCR[14] dictates whether the CellularRAM device is in variable or fixed latency mode. TN-45-22 defines the differences between variable and fixed latency.

Wait Pin Support

The WAIT pin is used to “flow control” the burst interface between the memory controller and the CellularRAM device. The CellularRAM device de-asserts the WAIT pin when it is ready to interface with the memory controller.

Memory Map/Chip Enable Considerations

A NOR Flash interface is designed to support a number of chip selects that can be configured to work with different device types. The CellularRAM device should use a separate chip enable (CE#) from the Flash device to ensure that it is not selected as the main boot device. This extra chip enable can be supplied either directly from the memory controller—typically referred to as a “non boot chip select”—or via the decode of the address outputs.

It should be noted that a “memory area” is associated with the chip select and that the modes of operation that are supported within this “memory area” need to match the controller/device driver. For example, the device driver must match the interface that both devices support (for example, burst READ/async WRITE, page READ/async WRITE) as well as other operational modes supported by the device, such as PAR or DPD. If there is a mismatch between the memory controller and the CellularRAM device, then undefined operations may occur.

Supply and I/O Voltage Support

The family of CellularRAM devices all support a 1.8V supply voltage and an I/O voltage in the range of 1.70–1.95V or 1.70–3.30V. The maximum I/O voltage depends on the CellularRAM device.

CellularRAM Hidden Refresh

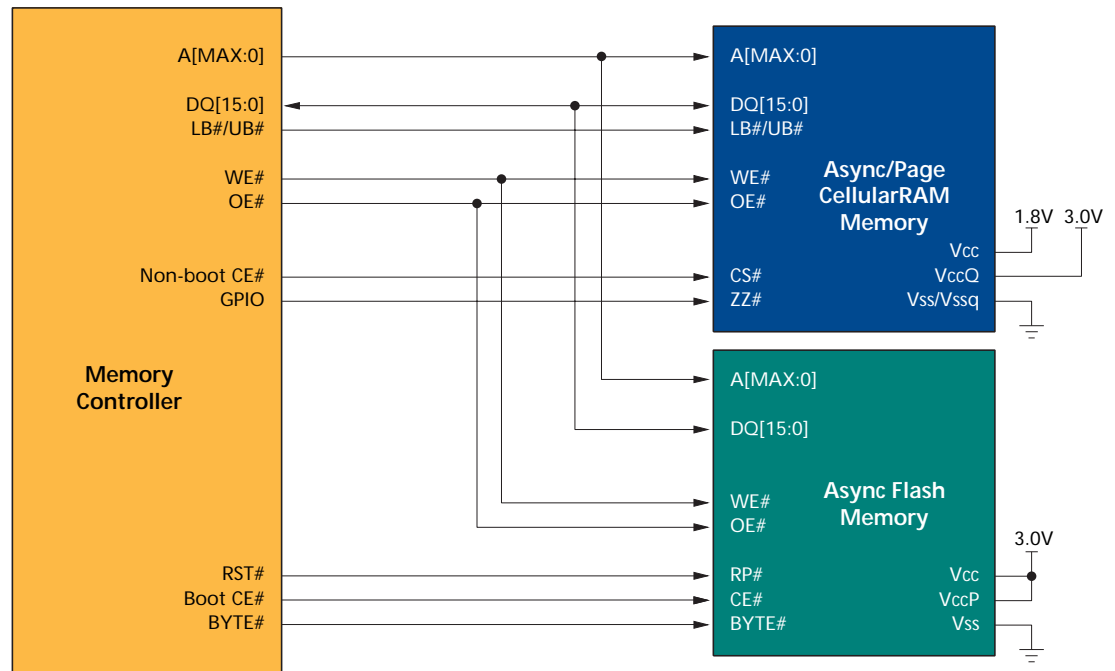
CellularRAM devices are based on DRAM technology, and unlike SRAM or Flash, refresh must occur at regular intervals (this refresh is hidden from the designer). This requirement is defined as $t_{CEM}^{(MAX)}$ and is the maximum time CE# can be asserted LOW. If t_{CEM} is violated, the memory contents become unstable and data loss may occur.

Connectivity Diagrams

This section provides basic connectivity block diagrams to clarify the connections between the NOR Flash memory controller and the CellularRAM device.

Async/Page Interface

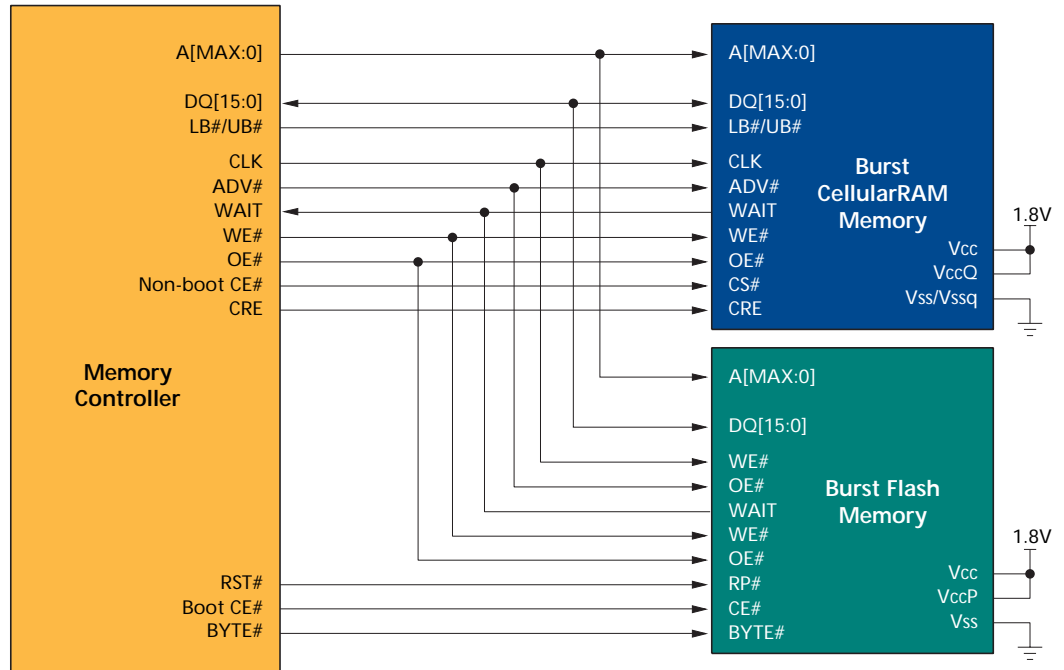
Figure 10: Async/Page CellularRAM Memory Controller



- Notes:
1. Vcc voltage may vary between the two memory devices, depending upon the device. The VccQ voltage of the devices must match.
 2. The memory controller must support a word-wide data bus.
 3. The CellularRAM device does not support a RP# connection.
 4. The chip selects must be separate, because the CellularRAM device cannot be the designated boot device.

Burst Interface

Figure 11: Burst CellularRAM Memory Controller



- Notes:
1. Vcc voltage may vary between the two memory devices, depending upon the device. The VccQ voltage of the devices must match.
 2. The CellularRAM device does not support a RP# connection.
 3. The memory controller does not have to support CRE.
 4. The chip selects must be separate, because the CellularRAM device cannot be the designated boot device.

Conclusion

The CellularRAM memory family of products are designed to work with a companion NOR Flash device and can support async/page, burst, or async/page/burst interfaces.

This technical note describes options and provides guidance on adding a CellularRAM device to a NOR Flash bus.

For further technical assistance, e-mail psramsupport@micron.com or visit Micron's Web site: www.micron.com/products/psram/.



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