

Technical Note

Fixed-Latency Operation in CellularRAM™ 1.0 Devices

Introduction

This technical note details how Micron has enhanced CellularRAM CR1.0 functionality to include fixed-latency operation. Fixed latency operation is not officially supported by the CellularRAM Workgroup in the CR1.0 specification.

For P23Z and P24A revision K devices in applications with a minimum 1.8V VCC, fixed-latency operation supports 43.8 MHz at a latency of 2, with a minimum setup time of 7ns to the processor. Frequencies between 43.8 MHz and 52 MHz require a latency of 3. The device does not support row boundary crossings in fixed-latency mode.

Fixed-Latency Support

The CR1.0 specification describes how the time to valid data changes during the initial latency of a burst READ or WRITE access, depending on whether or not the access occurs during a REFRESH cycle of the array. Fixed latency implies that each initial latency of a BURST READ or WRITE cycle will encounter valid data after a fixed delay from the start of a burst access.

Micron's CR1.0 devices are set to fixed-latency mode by writing to the bus configuration register (BCR). BCR[14] is listed in the CR1.0 specification as a reserved bit (the bit must be set to "0"). By changing BCR[14] to a "1," Micron CR1.0 devices function in fixed-latency mode until the bit is changed or the part is powered down. See Figure 1 on page 2 for detailed BCR information.

Figure 1: Bus Configuration Register Showing Initial Access Latency

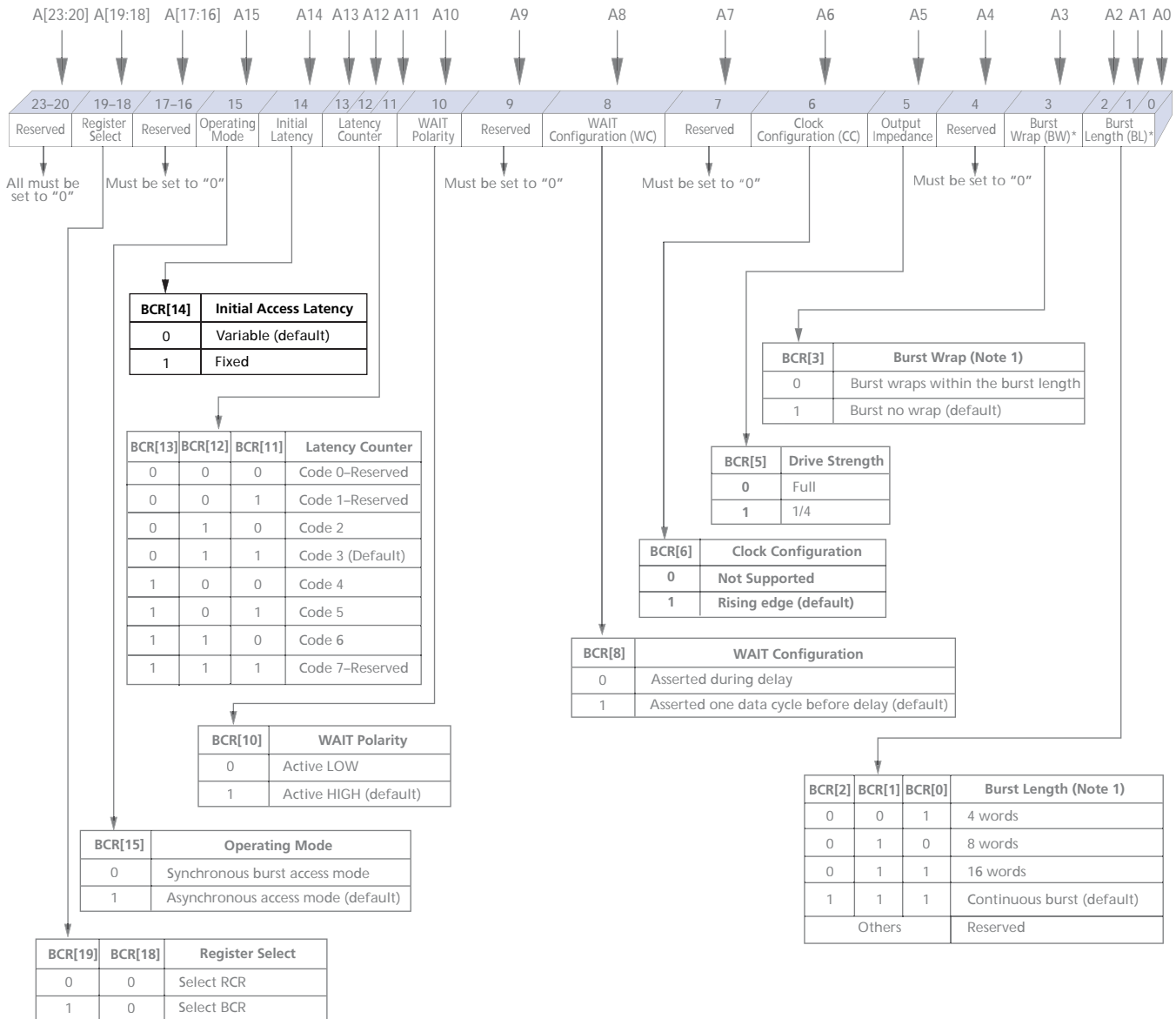


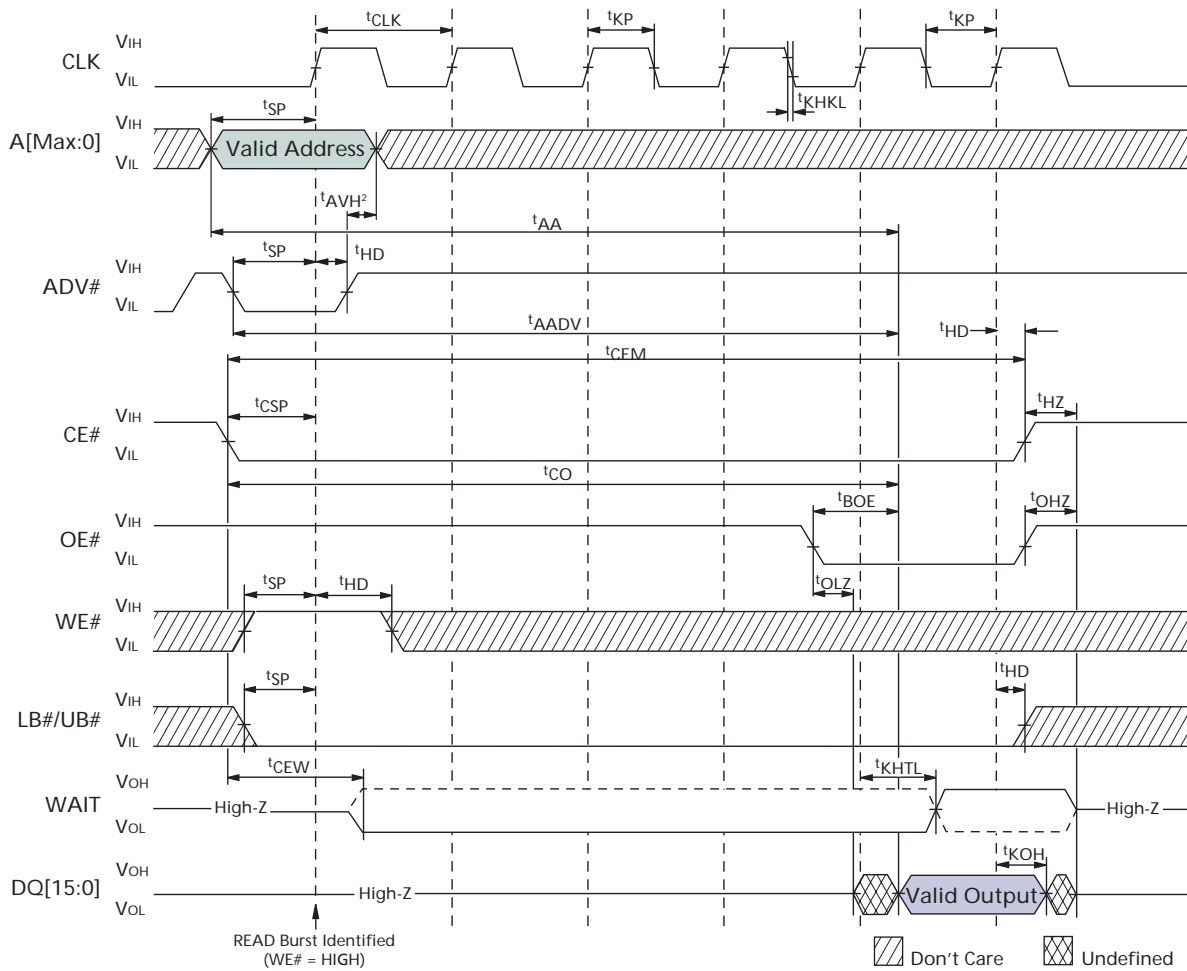
Table 2 shows the fixed-latency timing associated with the 32Mb MT45W2MW16BA and MT45W2MW16BP24A revision K die, as well as the 16Mb MT45W1MW16BD and MT45W1MW16BP23Z devices.

Table 2: Fixed-Latency Configuration for 16Mb (P23Z die) and 32Mb (P24A revision K die) Devices

| BCR[13:11] | Latency Configuration Code | Latency Count | Maximum Input CLK Frequency (MHz) | | |
|------------|----------------------------|---------------|-----------------------------------|-------------|-------------|
| | | | -701 ¹ | -708 | -856 |
| 010b | 2 (3 clocks) | 2 | 33 (30ns) | 33 (30ns) | 20 (50ns) |
| 011b | 3 (4 clocks) - Default | 3 | 52 (19.2ns) | 52 (19.2ns) | 33 (30ns) |
| 100b | 4 (5 clocks) | 4 | 66 (15ns) | 66 (15ns) | 40 (25ns) |
| 101b | 5 (6 clocks) | 5 | 75 (13.3ns) | 75 (13.3ns) | 52 (19.2ns) |
| 110b | 6 (7 clocks) | 6 | 104 (9.62ns) | 80 (12.5ns) | 66 (15ns) |
| Others | Reserved | - | - | - | - |

Notes: 1. The -701 (104 MHz speed grade) is only supported on the 16Mb device.

Figure 3: Timing Diagram for 16Mb (P23Z) and 32Mb (P24A revision K die) Including t_{AVH} Specifications



- Notes:
1. Non-default BCR settings: fixed latency; latency code 4 (5 clocks); WAIT active LOW; WAIT asserted during delay.
 2. $t_{AVH} = 2\text{ns}$ has been added to reflect the need to provide an address hold time from ADV# HIGH.

Enhanced Performance for LC=2 in Fixed latency

The maximum frequency supported for each latency code is listed in Tables 1 and 2. The AC timing and DC specifications for these devices are available from micron.com/products/psram/.

For P23Z and P24A Rev K, enhanced performance (43.8 MHz with LC=2) with a minimum 7ns setup time to the processor can be achieved if the application's VCC minimum does not go below 1.8V. See Table 3 for enhanced timing values.

Table 3: Enhanced Timing Values (valid for Vcc = 1.8V to 1.95V, fixed latency, LC=2)

| Symbol | Description | Enhanced Specifications | Data Sheet Specifications | Units |
|-----------------|---------------------------------------|-------------------------|---------------------------|-------|
| t_{CW} (MIN) | CE# to end of WRITE | 60 | 70 | ns |
| t_{AW} (MIN) | Address valid to end of WRITE | 60 | 70 | ns |
| t_{BW} (MIN) | UB#/LB# valid to end of WRITE | 50 | 70 | ns |
| t_{BA} (MIN) | UB#/LB# access time | 60 | 70 | ns |
| t_{SP} (MIN) | ADV#/Address setup time-to-clock | 9 | 3 | ns |
| t_{CSP} (MIN) | CE# setup time-to-clock (t_{CSP}) | 9 | 5 | ns |

- Notes:
1. Frequencies between 43.8 MHz and 52 MHz will require LC=3.
 2. The devices will not support row boundary crossings when fixed-latency mode is selected.

Summary

Micron CR1.0 devices support fixed-latency operation by setting BCR[14] to a "1." Fixed-latency operation supports 43.8 MHz at a latency of 2 with a minimum setup time of 7ns to the processor for applications with a minimum of 1.8V VCC.



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