

Technical Note

Using a Micron[®] CellularRAM[™] Device with the AMCC PPC405EZ Embedded Processor

Introduction

The Applied Micro Circuits Corporation (AMCC) PowerPC[®] 405EZ embedded 32-bit RISC processor provides an external memory bus that is specifically designed to interface with a x16 CellularRAM[™] device. This technical note describes the design requirements for a seamless memory connection between the PPC405EZ and a Micron[®] CellularRAM device.

Micron CellularRAM Overview

Micron CellularRAM devices are high-speed, pseudo-SRAM memory devices developed for low-power, portable applications. These devices, which use a DRAM-based memory core, are designed to be backward compatible with the more costly 6-transistor SRAM. For seamless operation on an SRAM bus, CellularRAM devices incorporate a transparent self refresh mechanism. This hidden refresh requires no additional support from the system memory controller and has no significant impact on READ/WRITE performance.

This technical note focuses on the asynchronous/page/burst, 128Mb, CellularRAM 1.5-compliant device, MT45W8MW16B. For more information on the device, refer to the MT45W8MW16BGX data sheet at www.micron.com/products/psram/partlist.

AMCC PowerPC 405EZ Overview

The AMCC PowerPC 405EZ is a system-on-a-chip solution for a wide range of applications including industrial control, test and measurement, commercial and retail systems, Internet appliances, and intelligent USB peripherals. It is a programmable, general-purpose, 32-bit RISC embedded processor. The PPC405EZ nonvolatile external memory interface supports both asynchronous and burst mode operations with a maximum clock rate of 83 MHz.

Power-up Considerations and Default Operational Mode

The CellularRAM device starts the internal initialization phase when the power supply rail reaches a valid power level ($V_{CC} = 1.7\text{--}1.95\text{V}$). At this point, the internal control circuitry begins to initialize, and the CellularRAM device will be available for the first access, $CE\# = \text{LOW}$.

Table 1: Initialization Time

Device	Time	Default Mode
Micron CellularRAM	150 μs (MAX)	Asynchronous

During this initialization phase, the CellularRAM device configuration register (CR) is loaded with its default data sheet values. The CellularRAM device powers up in a default asynchronous mode and must be reconfigured if burst mode operation is required.

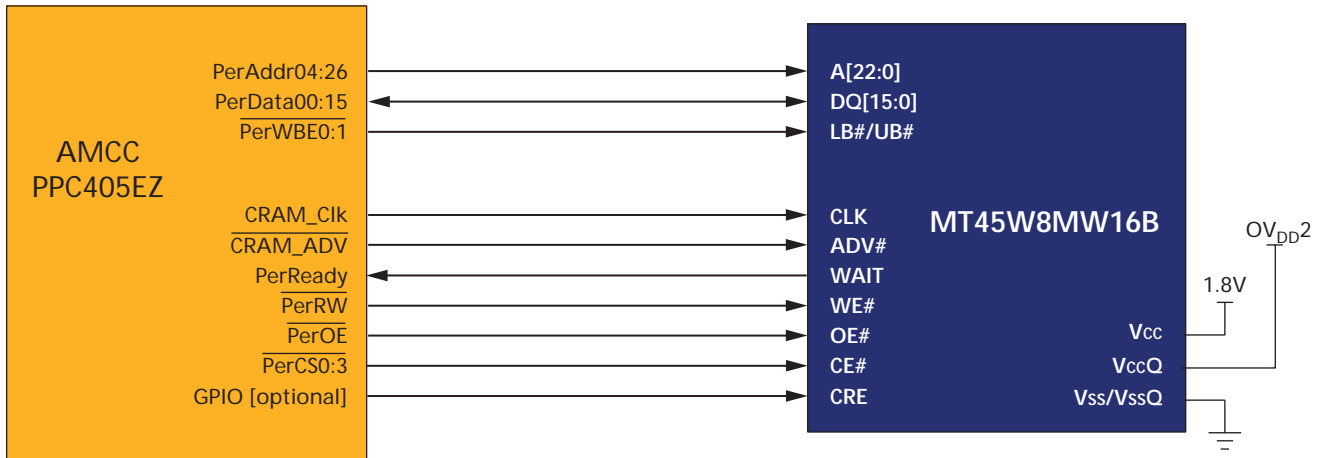
I/O Supply Voltage

The PPC405EZ external bus controller (EBC) output supply (OV_{DD2}) provides the I/O voltage to all devices on the external memory bus and is connected to the V_{CCQ} supply pin on the CellularRAM device. When interfacing with a CellularRAM device, the PPC405EZ requires that the I/O voltage be greater than 2.5V. Since the maximum limit on V_{CCQ} for the 128Mb CellularRAM device is 3.3V, the voltage range allowed on OV_{DD2} is 2.5–3.3V.

Block Diagrams

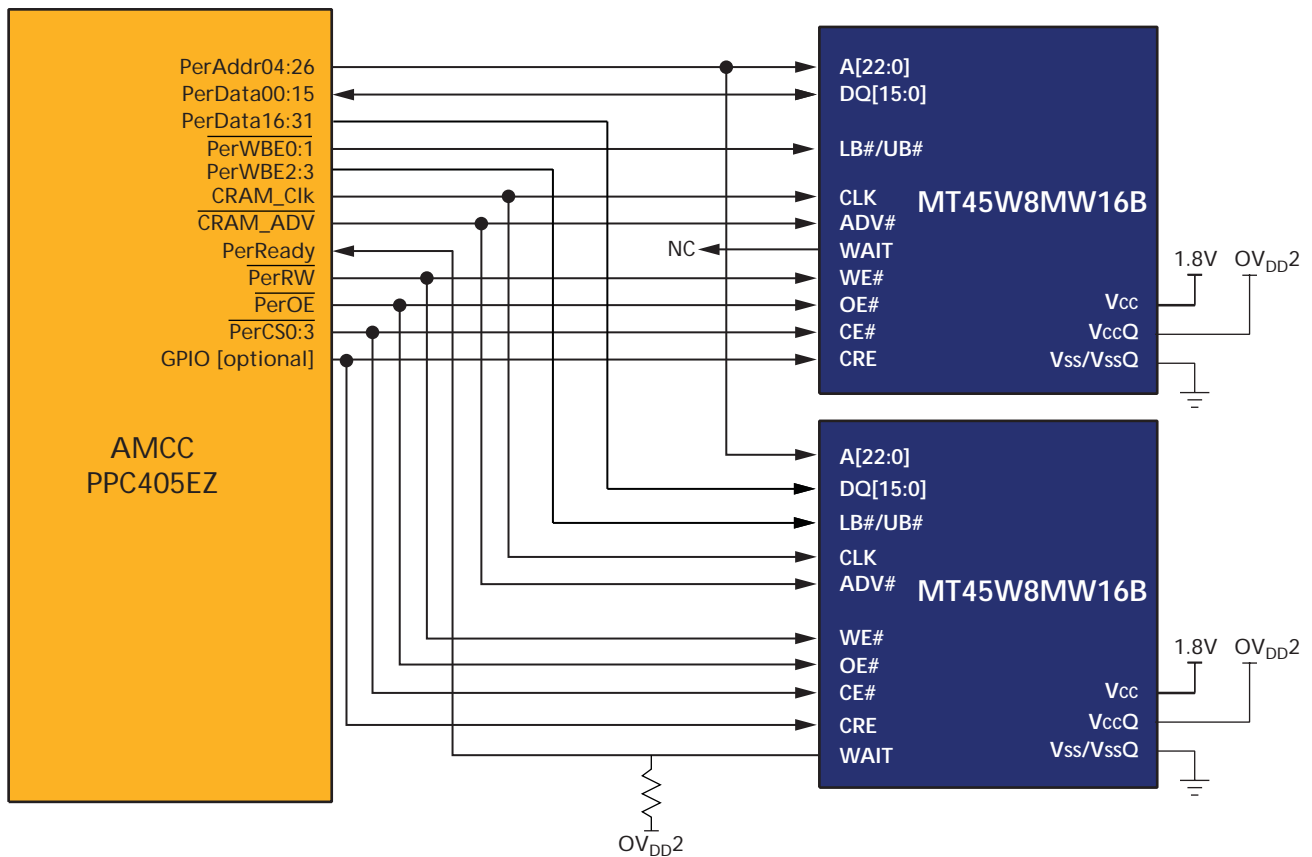
The connections between the PPC405EZ and the 128Mb burst mode CellularRAM device for a 16-bit external memory bus interface are shown in Figure 1 on page 3.

Figure 1: CellularRAM to PPC405EZ: 16-Bit Interface



Two CellularRAM devices can be combined to achieve a 32-bit memory interface, as shown in Figure 2. In this case, fixed latency is required in order to synchronize data flow to the processor. The WAIT pin of one of the devices is floated while the WAIT signal of the other device is monitored by the system memory controller.

Figure 2: CellularRAM to PPC405EZ: 32-Bit Interface



Deep Power-Down

For designs requiring very low standby current, the system designer will need to include control for the CellularRAM control register enable (CRE) pin via one of the general purpose I/Os available on the PPC405EZ. This will enable the CellularRAM device to enter deep power-down (DPD) mode.

Configuration Register Access

To configure the CellularRAM device, the design must access the bus configuration register (BCR) and the refresh configuration register (RCR). The access can be performed via a software access mode or a hardware access mode. To use the hardware access mode, the designer must use a PPC405EZ general-purpose input/output (GPIO) to control the Micron CellularRAM device CRE pin. Further details regarding configuration-register access are available in the Micron CellularRAM device data sheet.

Asynchronous Mode Operation

Both the CellularRAM and the PPC405EZ support asynchronous mode operations, which require that the signals listed in Table 2 be connected between the CellularRAM and the PPC405EZ EBC. Page mode operation is not supported on the PPC405EZ. This CellularRAM feature is automatically disabled on power-up and requires modification of the refresh configuration register to be enabled.

Table 2: Asynchronous Mode Signals

Signal Name	CellularRAM	PPC405EZ
Chip select	CE#	$\overline{\text{PerCS0:3}}$
Output enable	OE#	$\overline{\text{PerOE}}$
Write enable	WE#	PerRW
Byte enable	LB#/UB#	$\overline{\text{PerWBE0:1}}$
Address bus	A[22:0]	PerAddr04:26
Data bus	DQ[15:0]	PerData00:15

Asynchronous READ Operation

Figure 3 shows the timing diagram for the CellularRAM asynchronous READ operation. Table 3 shows the registers on the PPC405EZ that must be set in order to meet the CellularRAM READ timing requirements.

Figure 3: Asynchronous READ Timing

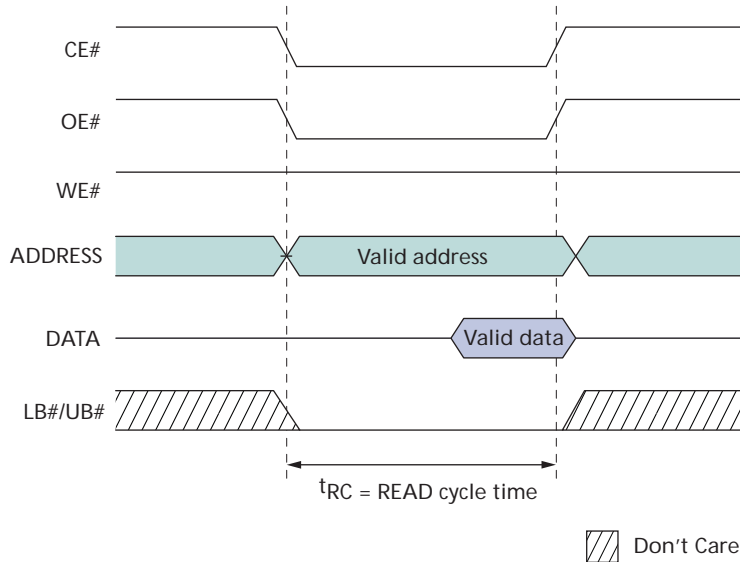


Table 3: Asynchronous READ Register Settings

Timing Description	PPC405EZ Register
CS#_LOW after valid address	EBC0_BnAP[CSN]
OE#_LOW after CS#_LOW	EBC0_BnAP[OEN]
Data read, CE# and OE#_HIGH	EBC0_BnAP[TWT] + 1 cycle
End of READ cycle hold time	EBC0_BnAP[TH]

Asynchronous WRITE Operation

Figure 4 shows the timing diagram for the CellularRAM asynchronous WRITE operation. WRITE timings on the PPC405EZ are WE#-controlled for byte-enabled mode and CE#-controlled for non-byte-enabled mode. The byte enable mode register, EBC0_BnAP[BEM], determines if the byte enable signals are active. Tables 4 and 5 show the registers on the PPC405EZ that must be set in order to meet the CellularRAM WRITE timing requirements for byte-mode and non-byte-mode operation.

Figure 4: Asynchronous WRITE Timing

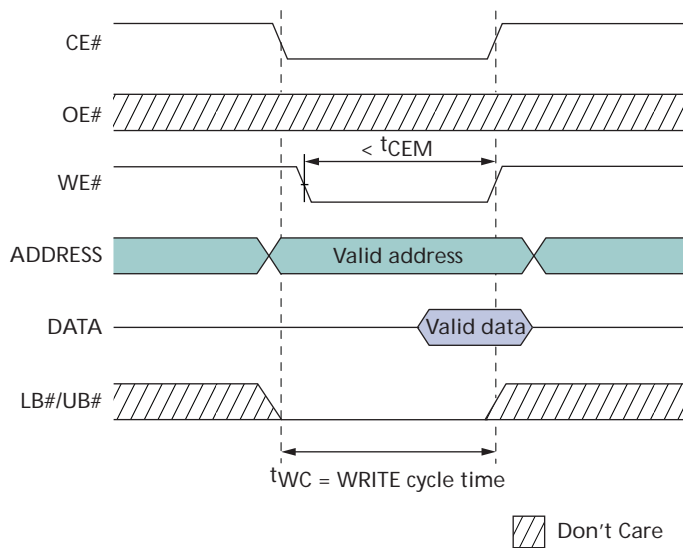


Table 4: Asynchronous Byte-Mode WRITE Timing Registers

Timing Description	PPC405EZ Register
Byte enable mode register (enabled)	EBC0_BnAP[BEM] = 1
CS#_LOW after valid address	EBC0_BnAP[CSN]
WE#, LB#/UB# LOW	EBC0_BnAP[WBN]
WE#, LB#/UB# HIGH	EBC0_BnAP[TWT] - [WBF] + 1 cycle
CE# driven HIGH	EBC0_BnAP[TWT] + 1 cycle
End of WRITE cycle hold time	EBC0_BnAP[TH]

Table 5: Asynchronous Non-Byte-Mode WRITE Timing Registers

Timing Description	PPC405EZ Register
Byte enable mode register (disabled)	EBC0_BnAP[BEM] = 0
WE#_LOW with valid address	NA
CS#_LOW after valid address	EBC0_BnAP[CSN]
CE# driven HIGH	EBC0_BnAP[TWT] + 1 cycle
End of WRITE cycle, WE#_HIGH	EBC0_BnAP[TH]

Burst Mode Operation

The PPC405EZ includes an interface specifically designed for the CellularRAM burst mode operation, which allows the memory subsystem to synchronously read and write data up to the maximum 83 MHz EBC clock speed. Since the burst timing requirements between the memory and the system memory controller are critical, care should be taken not to heavily load the PPC405EZ external peripheral interface if burst operation is desired. Burst mode is enabled on the PPC405EZ by the burst mode enable bit, EBC0_BnAP[BME]. When implementing burst mode on the CellularRAM device, a designer needs to be aware of three important considerations: burst length, WAIT behavior, and latency settings.

The size of the burst can be specified in the CellularRAM BCR as either fixed-length or continuous burst. Fixed-length bursts consist of 4, 8, 16, or 32 words. Continuous bursts have the ability to start at a specified address and burst through the entire memory array.

The WAIT output on the CellularRAM device, which requires a pull-up resistor for proper functionality, informs the processor when the memory is ready for READ or WRITE operations. The WAIT pin is asserted as soon as CE# goes LOW and is de-asserted to indicate when data is ready to be transferred into or out of the memory. WAIT is also asserted if the burst crosses the boundary between 128-word rows. To ensure maximum flexibility, the PPC405EZ supports row boundary crossing, as defined in Technical Note TN-45-15, "Row Boundary Crossing Functionality in CellularRAM™ Memory," available at download.micron.com/pdf/technotes/CellularRAM/tn4515.pdf. The PerReady input on the PPC405EZ is used to monitor the WAIT output of the CellularRAM device when the EBC0_BnAP[RE] register is set to "1."

Initial latency for the 128Mb CellularRAM device can be configured as either variable or fixed. While variable latency achieves the highest burst READ data rate, fixed latency supports burst mode operation without any WAIT-signal monitoring, provided that the controller monitors row boundary crossings. As noted previously, fixed latency is required when two CellularRAM devices are used to implement a 32-bit bus.

Other register settings necessary for PerReady input configuration are available in the PPC405EZ Preliminary User's Manual available at www.amcc.com/MyAMCC/retrieveDocument/PowerPC/405EZ/PPC405EZ_UM2021_v1_24.pdf.

Burst Mode Interface

In addition to the asynchronous signals listed in Table 2 on page 4, three additional signals—CLK, ADV#, and WAIT—are required for burst mode operation on the CellularRAM device. These three signals—CLK, ADV#, and WAIT—are available on the PPC405EZ external peripheral interface, as detailed in Table 6. When burst mode is enabled on the PPC405EZ, the CRAM_ADV# signal is automatically programmed to be active LOW for 1 clock cycle whenever CE# goes LOW.

Table 6: Burst Mode Signals

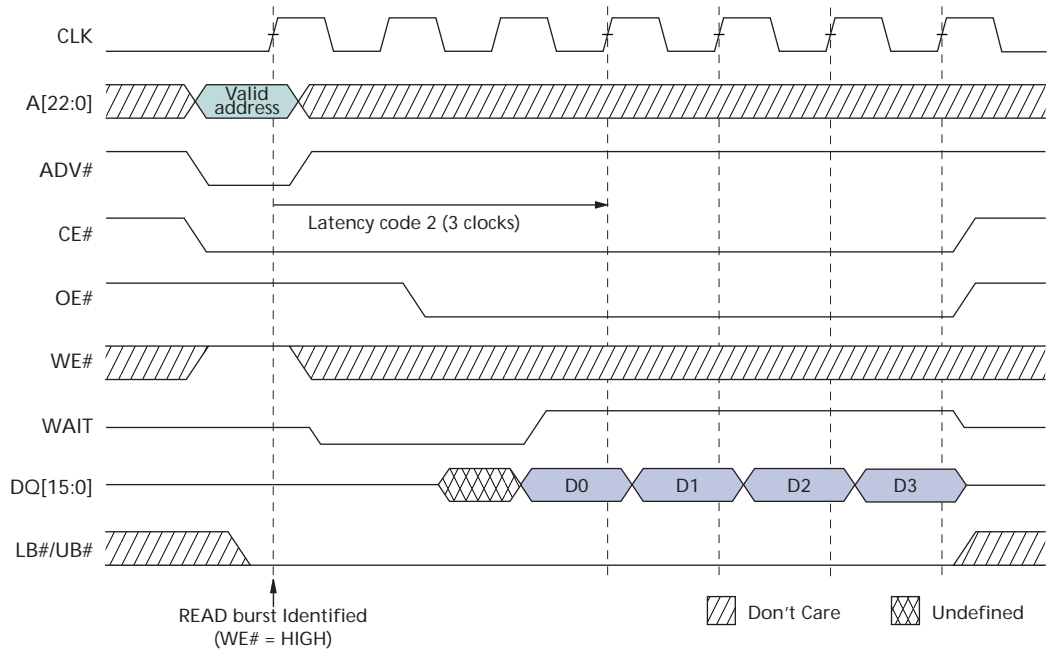
Signal Name	CellularRAM	PPC405EZ
Clock	CLK	CGRAM_Clk
Address valid	ADV#	CGRAM_AdV
WAIT	WAIT ¹	PerReady

Notes: 1. The CellularRAM device default configuration for WAIT-pin polarity is active HIGH (BCR[10] = 1), which matches the “asserted HIGH” requirement of the PPC405EZ PerReady input.

Burst READ Operation

Figure 5 shows the timing diagram for the CellularRAM Burst READ operation. Table 7 shows the register setting on the PPC405EZ needed to meet the CellularRAM burst timing requirements. For ease and simplification, only non-byte-mode burst READ and WRITE operations are covered in this technical note.

Figure 5: Burst READ Timing



A burst READ cycle begins when a valid address is clocked with ADV# LOW. OE# then transitions LOW according to register setting EBC0_BnAP[OEN]. The first data is read EBC0_BnAP[FWT] + 1 cycles after the start of the cycle as determined by the latency code setting on the CellularRAM device. The remaining addresses of the burst sequence are read out according to register setting EBC0_BnAP[BWT].

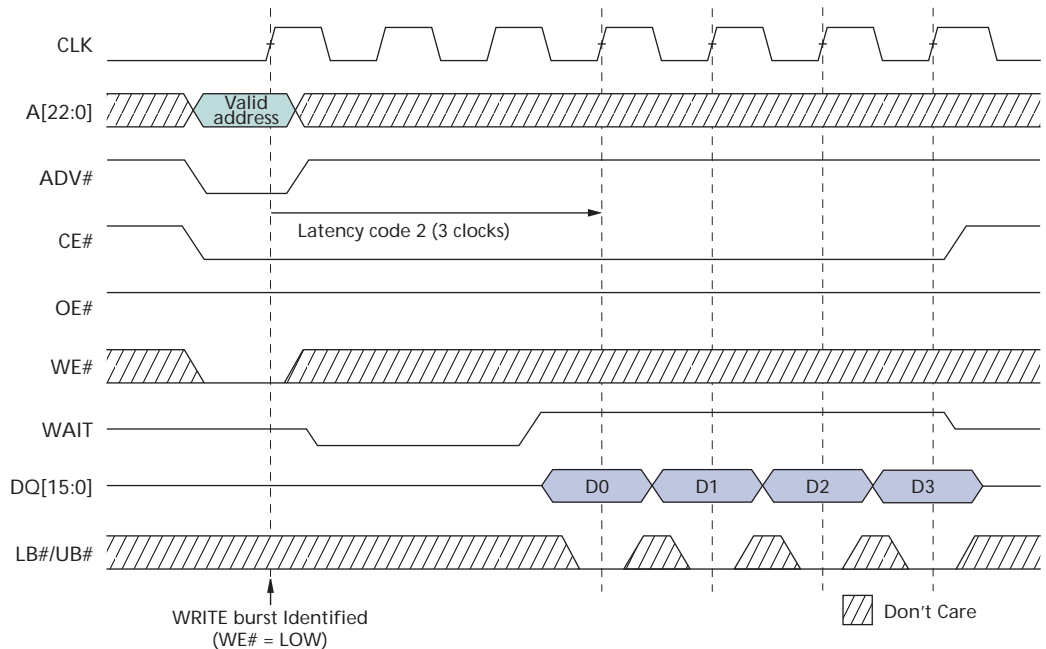
Table 7: Burst READ Timing Registers

Timing Description	PPC405EZ Register
Burst mode enabled	EBC0_BnAP[BME] = 1
Byte mode disabled	EBC0_BnAP[BEM] = 0
CS#_LOW after valid address	EBC0_BnAP[CSN]
ADV#_LOW for 1 cycle	Automatic when BME = 1
OE#_LOW after CS#_LOW	EBC0_BnAP[OEN]
First data read by processor	EBC0_BnAP[FWT] + 1 cycle
Remaining data in burst read	EBC0_BnAP[BWT] + 1 cycle
End of burst READ cycle hold time	EBC0_BnAP[TH]

Burst WRITE Operation

Figure 6 shows the timing diagram for the CellularRAM Burst WRITE operation. Table 8 shows the register setting on the PPC405EZ needed to meet the CellularRAM burst timing requirements.

Figure 6: Burst WRITE Timing



A burst WRITE cycle begins when a valid address is clocked with ADV# and WE# LOW. For non-byte-mode WRITES, the EBC waits for a number of clock cycles determined by register settings EBC0_BnAP[FWT] and EBC0_BnAP[WBF] to supply data for the first burst address. The controller writes to the remaining addresses of the burst sequence according to register setting EBC0_BnAOP[WBF].

Table 8: Burst WRITE Timing Registers

Timing Description	PPC405EZ Register
Burst mode enabled	EBC0_BnAP[BME] = 1
Byte mode disabled	EBC0_BnAP[BEM] = 0
CS#_LOW after valid address	EBC0_BnAP[CSN]
ADV#_LOW for 1 cycle after CS#_LOW	Automatic when BME = 1
WE#_LOW (same cycle as ADV#_LOW)	EBC0_BnAP[WBN]
First data written	EBC0_BnAP[FWT] + 1 - [WBF]
Remaining data in burst written	EBC0_BnAP[WBF]
End of burst READ cycle hold time	EBC0_BnAP[TH]

Memory Map

The PPC405EZ supports a maximum of eight memory devices connected to the EBC via the PerCS0:7 outputs. The recommended PPC405EZ chip select memory device connections are shown in Table 9.

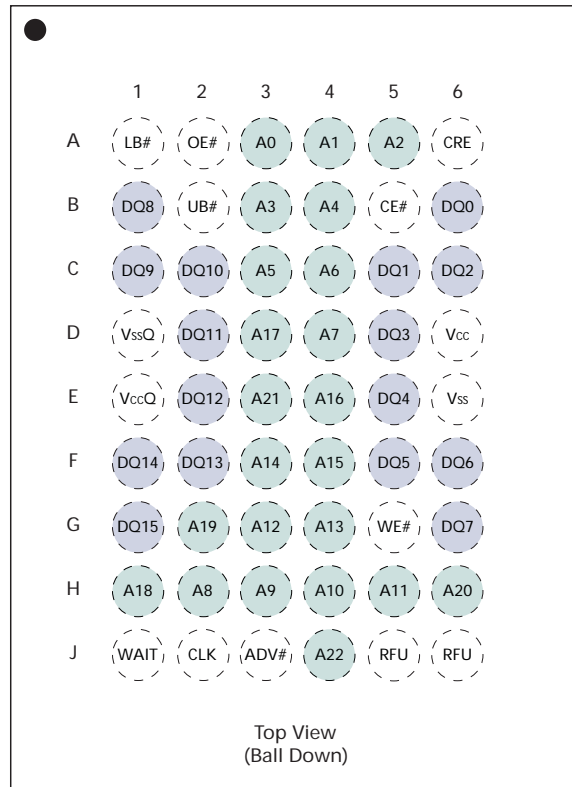
Table 9: PPC405EZ Chip Select Usage

PPC405EZ Chip Select	Recommended Device
$\overline{\text{PerCS0:3}}$	Micron CellularRAM (unless CS0 is needed for boot flash)
$\overline{\text{PerCS4}}$	Other memory device
$\overline{\text{PerCS5:7}}$	NAND Flash

CellularRAM Package Information

The Micron 128Mb burst CellularRAM device is available in a 54-ball VFBGA “green” package. The ball assignments for this package are shown in Figure 7.

Figure 7: 54-Ball VFBGA Ball Assignment



Summary

Micron CellularRAM devices offer both lower cost and seamless integration when used in place of traditional 6-transistor SRAM devices.

This technical note has provided guidelines for using Micron 128Mb CellularRAM devices with the AMCC PowerPC 405EZ embedded processor. Together, these products support both asynchronous and burst mode operations up to the maximum PPC405EZ clock frequency of 83 MHz. Timing and register setting details are available in the Micron MT45W8MW16B CellularRAM data sheet and the AMCC PPC405EZ data sheet and user's manual (see “References” on page 12).

For further technical assistance, e-mail psramsupport@micron.com or visit www.micron.com/products/psram/.

References

AMCC PowerPC 405EZ embedded processor preliminary data sheet:

[www.amcc.com/MyAMCC/retrieveDocument/PowerPC/405EZ/
PPC405EZ_DS2020_v1_26.pdf](http://www.amcc.com/MyAMCC/retrieveDocument/PowerPC/405EZ/PPC405EZ_DS2020_v1_26.pdf)

AMCC PowerPC 405EZ user's manual:

[www.amcc.com/MyAMCC/retrieveDocument/PowerPC/405EZ/
PPC405EZ_UM2021_v1_24.pdf](http://www.amcc.com/MyAMCC/retrieveDocument/PowerPC/405EZ/PPC405EZ_UM2021_v1_24.pdf)

Micron CellularRAM MT45W8MW16BGX data sheet:

www.micron.com/products/psram/partlist



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