

# Technical Note

## RLDRAM II Design Guide

### Introduction

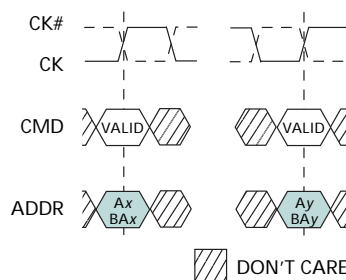
The Micron<sup>®</sup> Reduced Latency DRAM (RLDRAM II) addresses high-bandwidth memory requirements for communication data storage applications. The purpose of this design guide is to assist in establishing the general features of circuit implementations using this new device architecture.

RLDRAM II utilizes an 8-bank architecture optimized for high-speed operation and a double data rate I/O for increased bandwidth. The DDR interface transfers 36-, 18-, or 9-bit wide data words with programmable burst options of 2, 4, and 8, available to address a variety of applications (The burst of eight is on the x18 and x9 devices only). An on-chip delay-locked loop (DLL) and a free-running output data clock allow for better data capture schemes.

### Clocking Overview

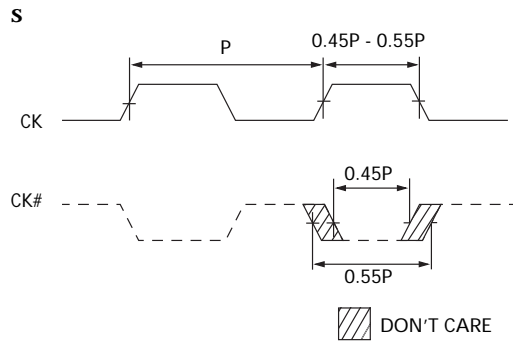
The RLD RAM II device requires a differential input master clock pair, CK and CK#. Ideally, CK and CK# are 180° out of phase, such that CK and CK# cross VREF at the same point. This balances the output data so that each data word has the same valid time. These signals may be generated directly by the controller chip or by a separate clock chip. Best system margins will be obtained when CK and CK# are exactly 180° out of phase. Only the rising edge of CK is utilized for address and control latching (see Figure 1). All timing specifications and diagrams in this technical note are examples; for accurate and complete information consult the current data sheet at [www.micron.com](http://www.micron.com).

**Figure 1: Address and Control Latching**



Ideally, the falling edge of CK (rising of CK#) occurs one-half clock cycle after the rising edge of CK (falling of CK#), but the individual duty cycle of CK and CK# can range from 45/55 to 55/45 (see Figure 2 on page 2), simplifying the task of generating the clocks.

Figure 2: Duty Cycle Requirement



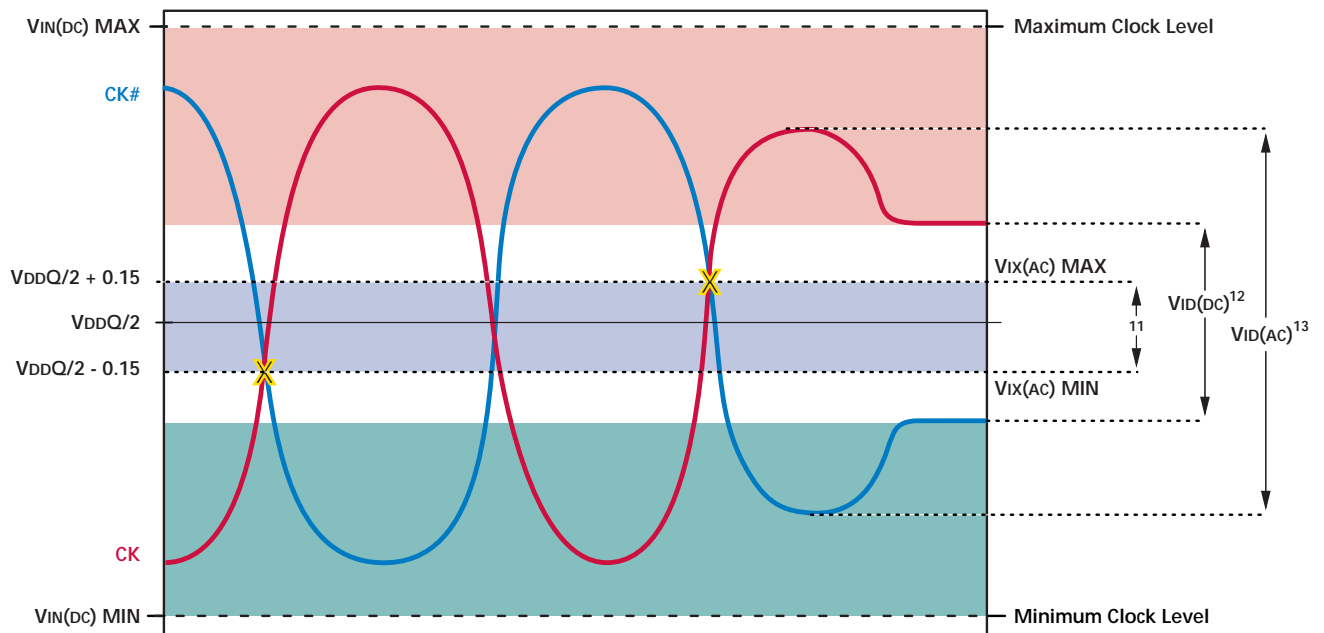
The specific crossing requirements between CK and CK# can be seen in Figure 3 on page 3.

RLDRAM II also requires a differential input data clock pair, DK and DK#. Both rising edges are utilized to latch in data to the device. Ideally, DK and DK# are 180° out of phase, providing the best margin on write data. For the x36 configuration, two differential input data clock pairs are available, with DQ0–DQ17 referenced to DK0 and DK0# and DQ18–DQ35 referenced to DK1 and DK1#. This allows for a tighter matching of data to data clock. Both the x9 and x18 devices have one pair (DK/DK#). The time from the crossing of CK and CK# and the crossing of DK and DK# may be no more than  $t_{CKDK}$  (for example, –300ps to 500ps for the -25 device). This limitation is necessary to ensure that output data is delivered before being overwritten by following data. It is possible to use CK and CK# for DK and DK#, but considerations need to be made due to the additional loading on the CK pair.

Table 1: Clock Input

Notes: 1–8

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input voltage level; CK and CK#	$V_{IN}(DC)$	-0.3	$V_{DDQ} + 0.3$	V	
Clock input differential voltage; CK and CK#	$V_{ID}(DC)$	0.2	$V_{DDQ} + 0.6$	V	9
Clock input differential voltage; CK and CK#	$V_{ID}(AC)$	0.4	$V_{DDQ} + 0.6$	V	9
Clock input crossing point voltage; CK and CK#	$V_{IX}(AC)$	$V_{DDQ}/2 - 0.15$	$V_{DDQ}/2 + 0.15$	V	10

**Figure 3: Clock Input**


- Notes:
1. DKx and DKx# have the same requirements as CK and CK#.
  2. All voltages referenced to Vss.
  3. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operations are tested for the full voltage range specified.
  4. Outputs (except for IDD measurements) measured with equivalent load.
  5. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are tested for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 2 V/ns in the range between VIL(AC) and VIH(AC).
  6. The AC and DC input level specifications are as defined in the HSTL Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
  7. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK/CK# is VREF.
  8. CK and CK# input slew rate must be  $\geq 2$  V/ns ( $\geq 4$  V/ns if measured differentially).
  9. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
  10. The value of Vix is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
  11. CK and CK# must cross within this region.
  12. CK and CK# must meet at least VID(DC) MIN when static and centered around VDDQ/2.
  13. Minimum peak-to-peak swing.

The last set of clocks is the output data clock pair, QK and QK#. During a READ from the device, QK and QK# are transmitted by the RLD RAM II and edge-aligned with the output data. For both the x36 and x18 configurations, QK0 and QK0# are aligned with the lower half of the data bits while QK1 and QK1# are aligned with the upper half of the data bits.

The timing between these clock pairs and the output data is represented by  $t_{\text{QKQ0}}$  and  $t_{\text{QKQ1}}$ , respectively. A looser  $t_{\text{QKQ}}$  specification allows for the possibility of using just one pair of output data clocks for both the x36 and x18. For the x9 configuration, all output data is aligned with QK0 and QK0#. Since QK and QK# are derived from CK and CK#, the individual duty cycle of CK and CK# will be transferred to QK and QK#, with a small additional error. The exact relationship between CK/CK# and QK/QK#, as well as QK/QK# and the output data, is specified in the RLD RAM II data sheet.

The use of true differential clocking on the RLD RAM II device allows for a larger timing budget, which becomes critical at higher speeds. Quicker edge detection is possible since the device is comparing two opposite signals to determine clock transitions. Timing skew due to impedance mismatching and/or difference in trace length and topology should be minimized to get the most out of this clocking scheme.

Another option for the differential clocking is to provide a single clock for each pair, while tying the inverted signal to VREF. This pseudodifferential option can effectively halve the number of clock signals required, which can be useful in systems using multiple RLD RAM II devices. The cost of using a single clock per pair is in the timing budget. Since clock transitions are referenced to a constant voltage rather than a differential signal, there is some derating.

## DLL Considerations

The RLD RAM II has an on-chip DLL to generate the edge-aligned data and output data clock signals. There are a few requirements for stable DLL operation. The clock source must provide an input to the device with a clock phase jitter, as specified in the RLD RAM II data sheet ( $t_{\text{CK\_var}} \leq 200\text{ps}$  for the 300 MHz device). This value is the maximum allowed variation from any one rising edge of the clock to the next rising edge of that same signal.

Any time the clock is stopped during normal operation, 1,024 cycles (5 $\mu\text{s}$  at 200 MHz operation) are required for stable DLL operation after a stable master clock signal resumes. This requirement also holds true whenever the mode register bit A7 is used to reset the DLL. However, during device power-up, there is a sufficient amount of time for the DLL to lock on the incoming clock, so no special considerations are required.

The minimum required frequency for stable DLL operation is the same for all configurations on the RLD RAM II device. This is shown in the data sheet as  $f_{\text{CK}}(\text{MIN})$  and is 175 MHz (5.7ns maximum cycle time). This constraint permits the design of an extremely low-jitter DLL. Although it is not guaranteed, it is possible to operate the device below the minimum frequency with the DLL enabled. At frequencies below the minimum clock cycle time, DLL jitter increases and eventually the DLL will not be able to maintain lock. As a result, the DLL is susceptible to noise; can alias, lose lock, relock, skip a clock, etc.; and can potentially cause the RLD RAM II to not output all the desired data cycle or cause the data to shift. For these frequencies, disabling the DLL RESET function in the mode register would result in more reliable output data. Although this affects the output data clock skew in regard to the master clock, QK-to-output times do not change.

Since the DLL will be affected by changes in the supply voltage, the average change in DC value of VDD must be constrained. VDD slew rate must be less than 0.1V (DC) per 50ns for DLL lock retention. A sudden change in the DC value of VDD is not acceptable.

## Address Bus

The RLD RAM II's address bus width is affected by more than the configuration (x9, x18, x36) of the device. The mode register can be set such that the RLD RAM II registers the entire address in one clock cycle (non-multiplexed address mode) or in two clock cycles (multiplexed address mode). Using the multiplexed address mode effectively halves the width of the address bus by registering a portion (Ax) of the address on the first clock cycle and then registers the remaining portion (Ay) of the address on the second clock cycle. When the multiplexed address mode is used, the command and bank address are registered on the first clock with Ax. See "Multiplexed Address Mode" on page 7 for more information.

Burst length (BL) is another influence on the address width as determined by the mode register. When the default setting of BL = 2 is used, one internal address bit is used to perform the burst operation. The remaining address bits (A[0:20] for the x9, A[0:19] for the x18, and A[0:18] for the x36) are used to control which two chunks of data are accessed. If the RLD RAM II is configured such that it has a burst of four, an additional address bit is used internally for the burst operation, and the most-significant external bit becomes a "Don't Care," effectively reducing the external address count by one. For the x9 and x18 devices, a BL = 8 option is also available. With this configuration selected, three address bits are used for the internal burst operation and the two most significant bits are "Don't Care" in the external address. Table 2 illustrates which address are used for each combination of configuration and BL for the 288Mb device.

**Table 2: Address Bus Usage**

Burst Length	Configuration		
	x36	x18	x9
BL = 2	18:0	19:0	20:0
BL = 4	17:0	18:0	19:0
BL = 8	NA	17:0	18:0

## Separate I/O vs. Common I/O

Both separate I/O (SIO) and common I/O (CIO) versions of the RLD RAM II are available. The SIO device has a separate READ and WRITE bus to eliminate bus turnaround cycles and contention, and is available in a x18 configuration. This gives the x18 SIO device 18 data inputs and 18 data outputs.

The CIO version is available in x9, x18, or x36 configurations and has a shared READ/WRITE port that requires one additional cycle to turn the bus around. The preferred version should provide an optimal compromise between performance and utilization.

Some systems require a near-term READ-to-WRITE ratio of 1:1. In this case, the SIO device can offer full bus utilization. Other systems operate with more of a data streaming approach in which the near-term bus operation is 100 percent READ or 100 percent WRITE, even though the long-term balance is closer to 50 percent (that is, 24 READs followed by 24 WRITEs). In this case, the use of the SIO device would not offer an optimal utilization of the bus. This case calls for the use of the CIO RLD RAM II, in which the input and output share the data bus. The bus turnaround reduces the efficiency of the device but provides better utilization than that of the SIO device in these situations.

## Refresh

The RLD RAM II requires its entire content to be refreshed every 32ms much like other DRAM architectures. AUTO REFRESH (AREF) initiates a refresh for the device and must be used each time a refresh is required. When initiating a refresh, only the bank address need be specified. Any value on the address bus during a refresh is ignored, with the address generated internally by the refresh controller. The die contains an internal controller that is initialized to a random starting point for each bank when the device is powered up. Each time the AREF command is performed, the RLD RAM II refreshes a portion of the bank based on this controller, after which a counter increments in preparation for the next AREF command to that bank. Each counter automatically wraps around any time the last location of a bank is reached. The controller cannot be reset without powering down the device. Since the user does not have to supply the refresh address, the address buffers are not used. This can be beneficial for power consumption since no input current is used on the address bus to switch address lines. The refresh command is similar to other commands with regards to row cycle time ( $t_{RC}$ ) and execution, but since it does not require a second address part in multiplexed address mode, the refresh command can always be applied in consecutive clock cycles.

## Bank Usage

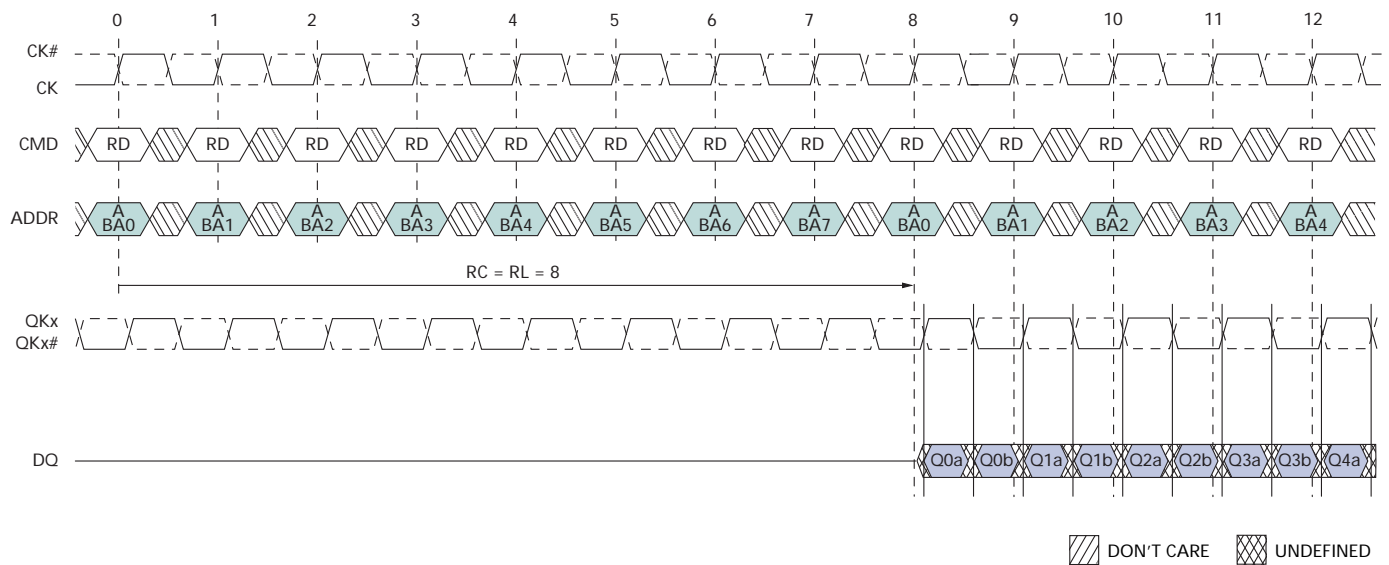
The incorporation of an 8-bank architecture allows the RLD RAM II to achieve its peak bandwidth by increasing the probability that a bank will be free. A relationship also exists between BL and the RLD RAM II configuration of the device and this probability. The mode register controls both BL and the RLD RAM II configuration. The selected  $t_{RC}$  defines how frequently any one bank can be accessed, while BL determines how often a new address is required. For instance, with a  $t_{RC}$  of four cycles and  $BL = 2$ , any one bank can be accessed every four clock cycles; on each clock cycle a new address is required, along with a minimum of 4 banks of memory, to sustain peak bandwidth. Banks can be accessed in any order at any time as long as the  $t_{RC}$  is met before revisiting a bank. To optimize the use of the 8-bank architecture, a round robin approach is recommended. This can be done by having the bank addresses as the least significant bits (LSBs) of the address, and then increment the LSBs in order to access each bank in sequence. The timing diagram in Figure 4 on page 7 demonstrates this approach. In cases where the access is more random, where the application does not allow such an approach, bank management becomes more critical. Table 3 illustrates the minimum number of banks that must be employed in order to have full bus utilization under a variety of conditions. The easiest example is 200 MHz, 8-word burst. In this case, one single access fills the data bus for four clock cycles. After four clock cycles ( $4 \times 5ns = 20ns$ ),  $t_{RC}$  is satisfied and all of the 8 banks are available. This is equivalent to having a 20ns SRAM, but with the low cost of DRAM technology.

Table 3: Bank Usage

Common I/O	-5	-3.3	-2.5
BL = 2	4	6	8
BL = 4	2	3	4
BL = 8	1	1/2 <sup>1</sup>	2

Notes: 1. Alternates between 1 and 2 each successive cycle.

Figure 4: Round Robin Example: 400 MHz Clock, Configuration 3



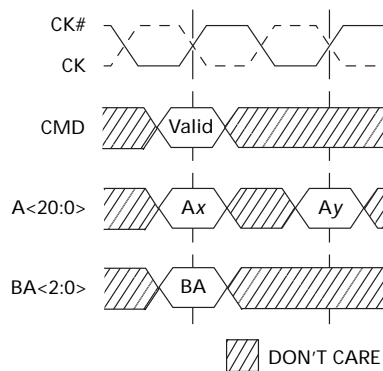
- Notes: 1. A/BAx: Address A of bank x  
 RD: READ  
 Dxy: Data y to bank x  
 RC: Row cycle time  
 RL: READ latency.

## Multiplexed Address Mode

Although the RLD RAM II has the ability to operate with a SRAM type interface by accepting the entire address in one clock, it can also be set in multiplexed address mode to latch the address more like a traditional DRAM device. In multiplexed address mode, the address presented to the RLD RAM II can be supplied in two consecutive clocks. This provides the advantage of reducing the number of pins required on the controller side by effectively halving the address pin count.

When using the multiplexed address mode, command and bank address are registered with the first address piece (Ax), as shown in Figure 5 on page 8. Figure 6 on page 9 demonstrates the address mapping scheme in multiplexed address mode and a method of connecting controller to RLD RAM II. On the following clock, the second piece of the address (Ay) is registered and the command is executed. This causes an increase of one clock cycle in the READ and WRITE latencies of the device in this mode, while the <sup>t</sup>RC remains the same. Multiplexed address mode also affects the efficiency of the device, but only when using the BL = 2 setting. This is due to the need for a new command on each clock for peak bus utilization, since only one clock cycle is required to read the data out of the memory when using BL = 2. The AREF command does not require a second address part, so it can be applied on consecutive clocks.

Figure 5: Command and Bank Latching in Multiplexed Mode



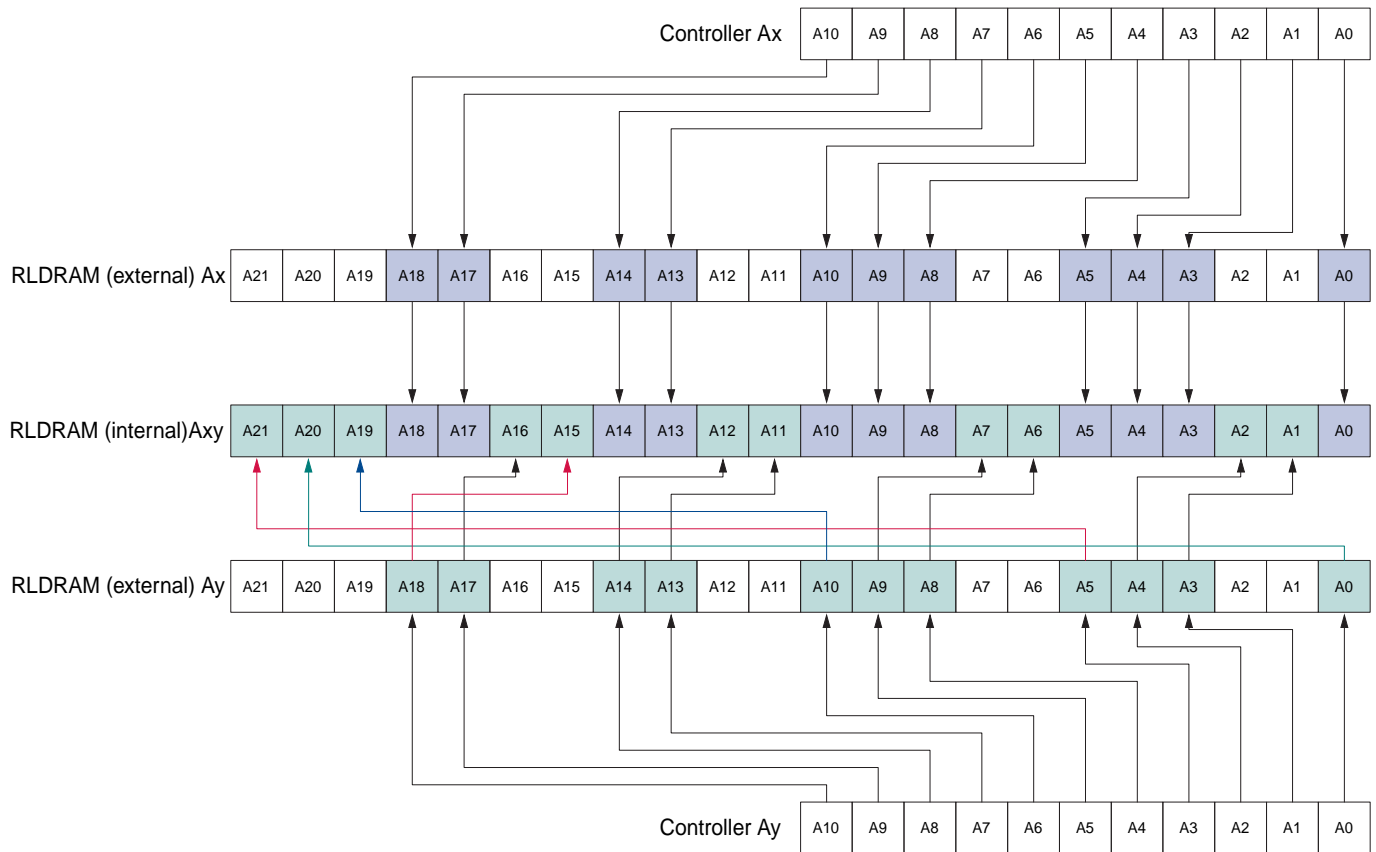
## Supply Voltages

Five sources ( $V_{DD}$ ,  $V_{EXT}$ ,  $V_{DDQ}$ ,  $V_{REF}$ ,  $V_{TT}$ ) provide the core, I/O, reference, and termination voltages required by the RLD RAM II. The core of the device requires a 2.5V  $V_{EXT}$  and 1.8V  $V_{DD}$ , while the output supply can be operated at nominal voltages of 1.5V or 1.8V as long as it does not exceed the level of  $V_{DD}$ . Both the reference voltage and the isolated termination supply are nominally one half of  $V_{DDQ}$ .

$V_{DD}$  and  $V_{EXT}$  must be applied prior to or concurrently with  $V_{DDQ}$ , with  $V_{REF}$  and  $V_{TT}$  applied at the same time as, or after,  $V_{DDQ}$ . There is no relationship between the sequence of  $V_{DD}$  and  $V_{EXT}$ , although the device will only start its power-up sequence after both voltages have reached their nominal levels. The clock may be supplied as soon as the supply voltages are stable. Once all voltages are stable, conditions need to be maintained for at least 200 $\mu$ s to guarantee stable device operation.

The RLD RAM II data sheet shows some of the requirements for the 2.5V  $V_{EXT}$  and 1.8V  $V_{DD}$  supplies while  $V_{DDQ}$  is very system dependent.  $V_{TT}$  is required for systems in which ODT is being used; otherwise, these pins may be connected to  $V_{DDQ}$  or left floating.  $V_{REF}$  is a very-low current source and can be achieved by a simple voltage divider.

Figure 6: Multiplexed Address Mode Mapping



## Initialization

Once the device is stable, issue two dummy MODE REGISTER SET (MRS) commands to train the device. Follow these with one valid MRS command to set the mode register. If address multiplexing is desired, issue an additional MRS command <sup>t</sup>MRSC after the valid MRS command in order to load Ax and Ay parts of the mode register bitmap. After the mode register is loaded and an additional <sup>t</sup>MRSC has passed, issue a refresh command to all 8 banks, in any order, with 2,048 cycles separating a refresh to each bank. Once all banks have been refreshed, <sup>t</sup>RC is required before the device is ready for normal operation.

**Note:** Always consult the latest data sheet for specified timing relationships on all timings discussed in this article.

## Depth/Width Expansion

The combination of several RLD RAM II devices on the same bus to achieve larger densities is made possible by the use of a small set of control signals, achieving both depth and width expansion by adding a few additional pins to the device controller. Due to the pin assignment of the RLD RAM II device, clamshell designs (which locate two devices on opposite sides of a PCB) are supported for both depth and width expansion. For both expansion methods, a few signals are required to be interrupted by vias, with different signals for each one.

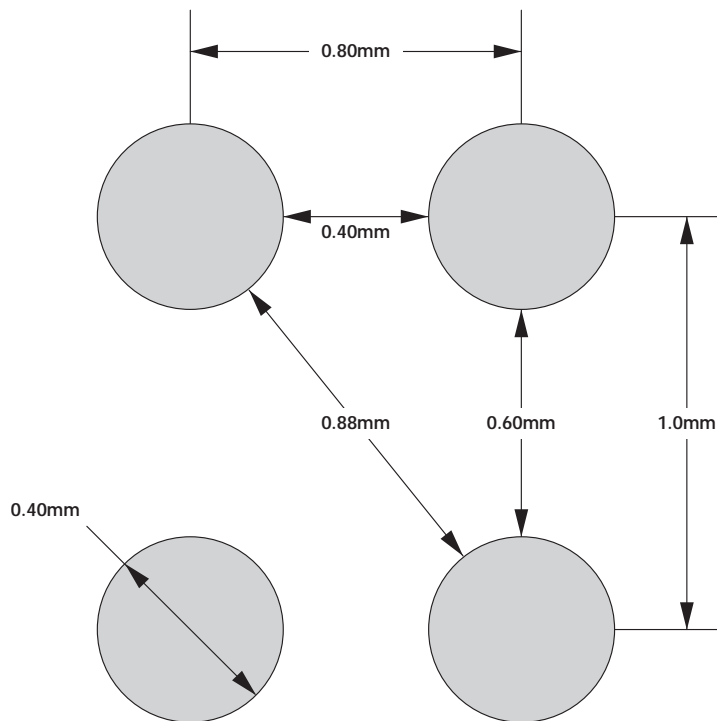
The address bus, data bus, input clocks, and all control signals except the chip select (CS#) are common when implementing depth expansion. Combining devices in ranks to give the appearance of one deeper RLD RAM II is easily achieved with the use of the CS# signal to select between the devices, with a goal to allow zero-wait-state transitions from one RLD RAM II to another in a different rank. At higher clock frequencies, one wait state could become necessary to avoid bus contention. Process, voltage, and temperature variations are eliminated by the DLL. However, there will be jitter differences between devices, a concern regarding bus contention if using a clamshell design. Even though two parts must meet the same parameters on the data sheet, there is no guarantee that one part cannot be much faster. In all practicality, voltage will be the same for two parts in close proximity to each other and this should hold true for temperature, as long as the average duty cycle of the parts is approximately the same. The data sheet specifies the maximum contention time to be  $2 \times t_{QKQ}(\text{MAX})$ . This measurement includes tester guardband, as well as allowances, by taking measurements at the fast corner (low temperature, high voltage) for data hold characteristics and at the slow corner (high temperature, low voltage) for data setup characteristics for the device. Clamshell designs are the best method of reducing the delay path between two devices and minimizing or possibly eliminating bus contention when switching between ranks.

Having more than two devices makes managing the delay path much more difficult and may require the addition of a wait state when switching between ranks. In these cases, careful analysis is required to determine the best way to achieve an acceptable amount of bus contention or the need for inserting a wait state to avoid it all together. The exact number of ranks that are possible with the RLD RAM II device is application dependent. The clock-generating ability and pin-to-pin skew of the controller all influence this value as well as the clock frequency of the application. Simulation is one of the best methods for determining this number.

Width expansion is generally an easier method of combining devices to increase memory size. The address bus, input clocks, and control lines are common in this scheme, while the data bus and output clocks are not shared. Greater bandwidth is achieved by placing additional devices in parallel, effectively increasing the size of the data bus. The operation of several devices in parallel to achieve the appearance of a single, wider device, is similar to that of the operation of a single RLD RAM II device with additional data lines. As more devices are added, there is a point at which the loading on the clock and control signals becomes an issue. With the use of simulation tools, the amount of loading that a single signal from the controller is able to support can be determined. Replicated signals can be used to increase this amount by reducing the load on any one signal while the data bus remains point-to-point with no additional loading.

## Board Layout Considerations

When using a BGA package, there are numerous schemes that can be implemented to route all signals on the system board while minimizing PCB complexity and cost. With variations in individual PCB design rules, providing a specific layout for all situations is impractical if not impossible. In order to use the RLD RAM II's 144-ball FBGA package, the user's PCB layout must have enough room for vias and escape routing to provide electrical connections to all relevant signals of the device. Figure 7 on page 11 gives an example of a surface landing pad layout—assuming landing pad size of 0.40mm (15.748 mils)—and shows the amount of space available for vias and escape routing to the signals of the RLD RAM II.

**Figure 7: Landing Pad Layout**


## Impedance Considerations

The RLD RAM II is equipped with programmable impedance output buffers to allow user-programmable output impedance control. This is accomplished with the use of a single resistor (R<sub>Q</sub>) connected between the ZQ pin and ground. The value of R<sub>Q</sub> should be five times the desired output impedance. The range allowed for R<sub>Q</sub> is 125Ω to 300Ω, which guarantees output impedance in the range of 25Ω to 60Ω (within 15 percent), along with the external resistor tolerance, which also translates to the output impedance setting. The RLD RAM II device periodically samples the value of R<sub>Q</sub> and transparently updates the impedance without affecting device operation. These updates compensate for variations in supply voltage and temperature that may occur over time. If ZQ is tied directly to ground, the minimum impedance is invoked while ZQ tied directly to V<sub>DD</sub> forces the maximum impedance. The mode register bitmap is used during power-up of the device to enable the programmable impedance function.

In order to keep like signals as similar in impedance as possible, the designer must pay close attention to the layout. There are many good tools that will perform simulations based on actual PCB layout. It is useful to design it from the outset rather than simulate the end result and see what happens. To that end, calculating the effects of some common layout conditions and discontinuities is useful to help the user know what to avoid. For convenience, a few equations are provided (see Equation 1). The equations are taken from Wadell's *Transmission Line Design Handbook*.<sup>1</sup>

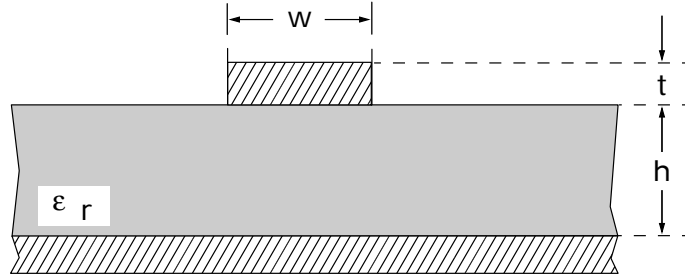
$$t_p = 1 \times \sqrt{\frac{\epsilon_{eff}}{c}} \quad (\text{EQ 1})$$

**Note:** If you prefer inches, c = 1.18E0 inches, and 1 is the length in inches.

Especially noteworthy are simple geometry changes to circuit board traces to match impedances, for example, using 90° mitered bends instead of plain 90° bends. These considerations are discussed to impress upon the reader the detailed attention required when making 500+ MHz buses function reliably.

The most common structure is the microstrip line shown in Figure 8. The most accurate equation for impedance is shown in Equation 2.

Figure 8: Microstrip Line



$$Z_0 = \frac{60}{\sqrt{2} \sqrt{\epsilon_{eff} + 1}} \ln \left( 1 + \frac{4h}{w'} \frac{14 + \frac{8}{\epsilon_{eff}}}{11} + \sqrt{\left( \frac{14 + \frac{8}{\epsilon_{eff}}}{11} \right)^2 \left( \frac{4h}{w'} \right)^2 + \frac{1 + \frac{1}{\epsilon_{eff}}}{2} \pi^2} \right)$$

$$\text{Where } \epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[ \sqrt{1 + \frac{12h}{w'}} + 0.04 \left( 1 - \frac{w}{h} \right)^2 \right] \text{ for } \frac{w}{h} < 1$$

$$\text{Where } \epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[ \sqrt{1 + \frac{12h}{w'}} \right] \text{ for } \frac{w}{h} \geq 1$$

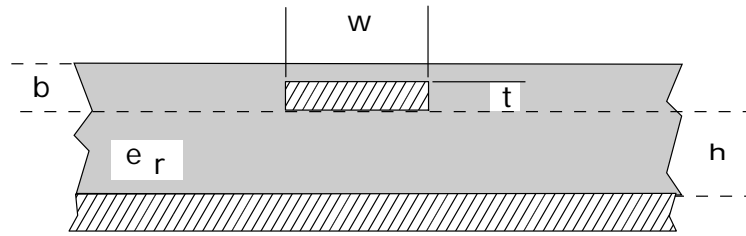
$$w' = \left[ \frac{1 + \frac{1}{\epsilon_{eff}}}{2} \right] \frac{t}{\pi} \times \ln \left[ \frac{4\epsilon_{eff}}{\sqrt{\left( \frac{t}{h} \right)^2 + \left( \frac{t/\pi}{w/(t+1.1)} \right)^2}} \right] \quad (\text{EQ 2})$$

In multilayer PCBs, embedded (or buried) microstrip lines are often encountered. This is shown in Figure 9 on page 13. Impedance is calculated as in Equation 2 but with a correction:

$$Z_0 = Z_{0, \text{microstrip}} \frac{\sqrt{\epsilon_{eff, \text{microstrip}}}}{\sqrt{\epsilon_{eff, \text{buried}}}}$$

$$\text{Where } \epsilon_{eff, \text{buried}} = \epsilon_{eff} e^{\left( -\frac{2b}{h} \right)} + \left[ 1 - e^{\left( -\frac{2b}{h} \right)} \right] \quad (\text{EQ 3})$$

Figure 9: Buried Microstrip Line



A microstrip line bend (Figure 10) is modeled as an L-C-L network with these values:

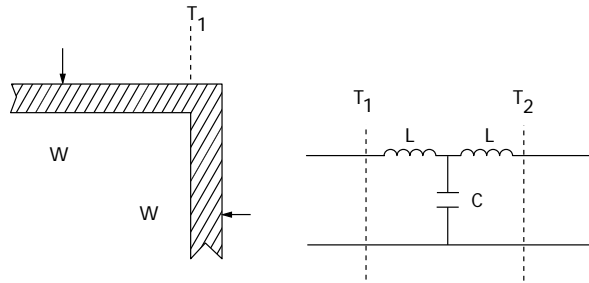
$$L = 50h \left( 4 \sqrt{\frac{w}{h}} - 4.21 \right) nH$$

$$C = \frac{w}{\sqrt{\frac{w}{h}}} (14\epsilon_r + 12.5) \left( \frac{w}{h} - 1.83\epsilon_r + 2.25 \right) + 0.02\epsilon_r h [pF] \text{ for } \frac{w}{h} < 1$$

$$C = w \left( (9.5\epsilon_r + 1.25) \frac{w}{h} + 5.2\epsilon_r + 7.0 \right) [pF] \text{ for } \frac{w}{h} \geq 1$$

(EQ 4)

Figure 10: Microstrip Line Bend



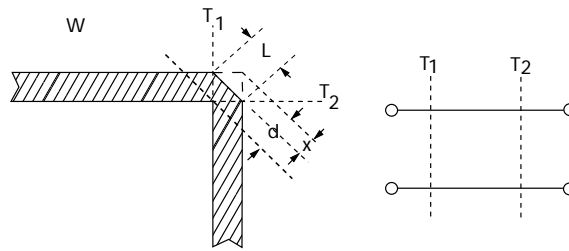
This bend can be impedance-matched to the rest of the metal trace by using an optimal right-angle mitered bend (as shown in Figure 9) and the matched impedance equation:

$$L = w\sqrt{2} \left[ 1.04 + 1.3e^{\left(-1.35\frac{w}{h}\right)} \right]$$

$$d = x + \sqrt{2}w - \frac{L}{2}$$

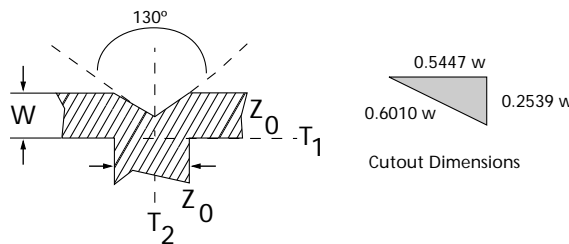
(EQ 5)

Figure 11: Buried Microstrip Line



Likewise, a microstrip line T junction introduces a discontinuity. The solution for matching impedance is shown in Figure 12. The cut-out triangle dimensions are supplied in the figure.

Figure 12: Microstrip Line T Junction



Vias are also important sources of discontinuities. For a discussion on designing a via for a desired impedance, see Wang, Taoyun, et al., “Quasi-static Analysis of a Microstrip Via Through a Hole in a Ground Plane.”<sup>2</sup>

## Bypass Capacitor Selection

Micron recommends using a minimum of two (and ideally three or four) low-inductance 0.1  $\mu\text{F}$  ceramic capacitors from  $V_{DD}$  to  $V_{SS}$  planes, located near the RLD RAM II. See Micron Technical Note TN-00-06, “Bypass Capacitor Selection,” for more details.  $V_{DDQ}$  is less important to bypass, but it is recommended to add two low-inductance 0.1  $\mu\text{F}$  ceramic capacitors from  $V_{DDQ}$  to  $V_{SS}$  planes, located near the RLD RAM II.

## HSTL Inputs

RLDRAM II inputs conform to the JEDEC HSTL standard.  $V_{DDQ}$  is specified at 1.5V nominal. It is acceptable to operate the device with  $V_{DDQ}$  at 1.8V nominal to permit direct interfacing with 1.8V logic components. Operating at the higher  $V_{DDQ}$  will result in elevated I/O power.

The designer has freedom to set  $V_{REF}$  to any value within the allowed device tolerance. The optimal  $V_{REF}$  value is the middle of the “clean zone” between the top of the ground noise floor and the bottom of the supply noise floor. This often is not  $V_{DDQ}/2$  but some slightly higher value.  $V_{REF}$  consumes very little current. Use a resistor divider ( $V_{DDQ}$  to  $V_{SS}$ ) with parallel capacitance as near to the RLD RAM II as possible and guard the  $V_{REF}$  PCB traces with ground traces where possible.  $V_{REF}$  also can be biased to compensate for differences in the ASIC driver’s HIGH-to-LOW versus LOW-to-HIGH slow rates. If, for example, the RLD RAM II is controlled by the ASIC, which drives HIGH-to-LOW in 1ns

but LOW-to-HIGH in 1.2ns, it takes 0.5ns to drive LOW, but 0.6ns to drive HIGH. Adjusting VREF to a value less than midrail will restore this balance to 0.55ns in each direction.

The receivers on the RLD RAM II use VREF as the logic “1” vs. “0” reference point.

## References

1. Wadell, Brian C. (1991) *Transmission Line Design Handbook*. Norwood: Artach Honte, Inc.® 1991.
2. Wang, Taoyun, et al., “Quasi Static Analysis of Microstrip Via Through a Hole in a Ground Plane,” *IEEE Transactions on Microwave Theory and Techniques*. Vol. MTT-36, No. 6. June 1988, pp. 1007–1013.



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