

# Technical Note

## RLDRAM<sup>®</sup> II Clocking Strategies

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### Introduction

The Micron<sup>®</sup> reduced latency DRAM II (RLDRAM<sup>®</sup> II) addresses the high-bandwidth memory requirements for communication and data storage applications. This is achieved through the use of a flexible clocking strategy that incorporates a series of clock pairs for managing both input and output data. A delay-lock loop (DLL) is utilized to synchronize output data.

The RLD RAM II device requires a differential input master clock pair, CK and CK#, and differential input data clock pairs, DK<sub>x</sub> and DK<sub>x</sub>#. The RLD RAM II has output data clock pairs, QK<sub>x</sub> and QK<sub>x</sub>#, that are derived from the input master clock pair.

For complete details regarding RLD RAM II, consult Micron's component data sheets and technical note "TN-49-01: RLD RAM II Design Guide," located on Micron's Web site: [www.micron.com](http://www.micron.com).

This technical note addresses the operation of the device outside the specified range of clock periods and the timing changes that occur in this mode of operation. It also addresses the possibility of running the device within the specified range of <sup>t</sup>CK with the DLL off (although closing timing could become a concern).

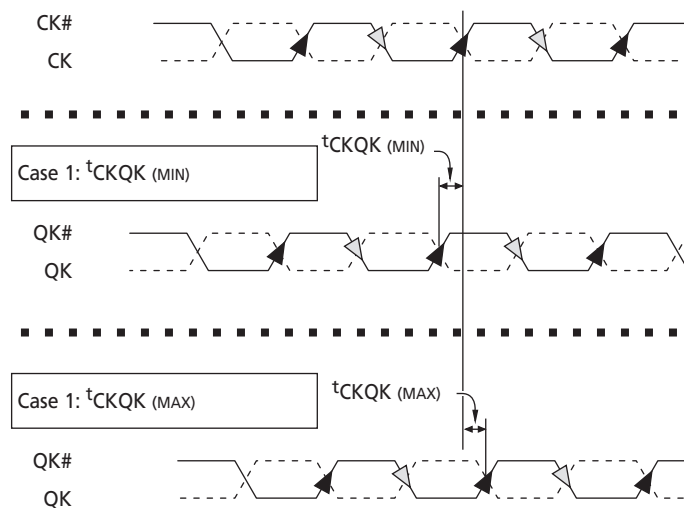
### DLL Considerations

The RLD RAM II device has an on-chip DLL to generate the edge-aligned data and output data clock signals. This results in a minimum required frequency for stable DLL operation for all configurations on the RLD RAM II device. This is shown in the data sheet as <sup>t</sup>CK (MAX). At frequencies below the minimum clock cycle time, the DLL delay becomes too great, eventually resulting in the DLL being unable to maintain lock. As a result, the DLL is susceptible to noise, can alias, lose lock, re-lock, skip a clock, etc.—potentially causing the RLD RAM II device to not output the entire desired data cycle, and certainly causing the data to shift. For these frequencies, using the DLL RESET (disable) function of the mode register would result in more reliable output data. Although this affects the output data clock skew in regard to the master clock, QK to output data times do not change.

## Operating the DLL Outside the AC Timing Specification

During initial system debug it is common to run the system much more slowly so events can be more easily captured. The RLD RAM II device employs a mode register bit that can select between enabling or disabling the DLL (default is disabled). The data sheet shows the safe value of the clock period in which the device can operate with the DLL enabled. Any operation below this range must be done with the DLL disabled. Figure 1 shows the timing relationship between CK and QK for the RLD RAM II device during normal operation, while Figure 2 demonstrates the effects on the  $t_{CKQK}$  timing with the DLL disabled. No change occurs in the relationship between QK and the output data when the DLL is disabled.

**Figure 1: Clock-to-Output Data Clock Timing with the DLL Enabled**



**Figure 2: Clock-to-Output Data Clock Timing with the DLL Disabled**

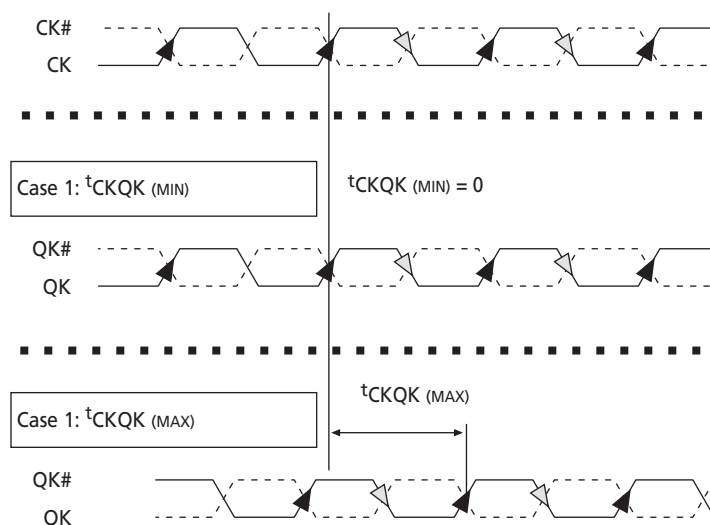


Table 1 shows the timing parameters for the various speed grades of the RLD RAM II device with and without the DLL enabled. Note the  $t_{CK}$  (DLL enabled) parameter for all speed grades. The RLD RAM II device can be operated in this range while achieving the  $t_{CKQK}$  (DLL enabled) parameter. Operation below this frequency range requires the DLL to be disabled due to a dead band of frequencies in which the DLL is unable to retain lock, at which time the  $t_{CKQK}$  (DLL disabled) parameter is met. Note also that no other timing parameters change when the DLL is disabled on the RLD RAM II device.

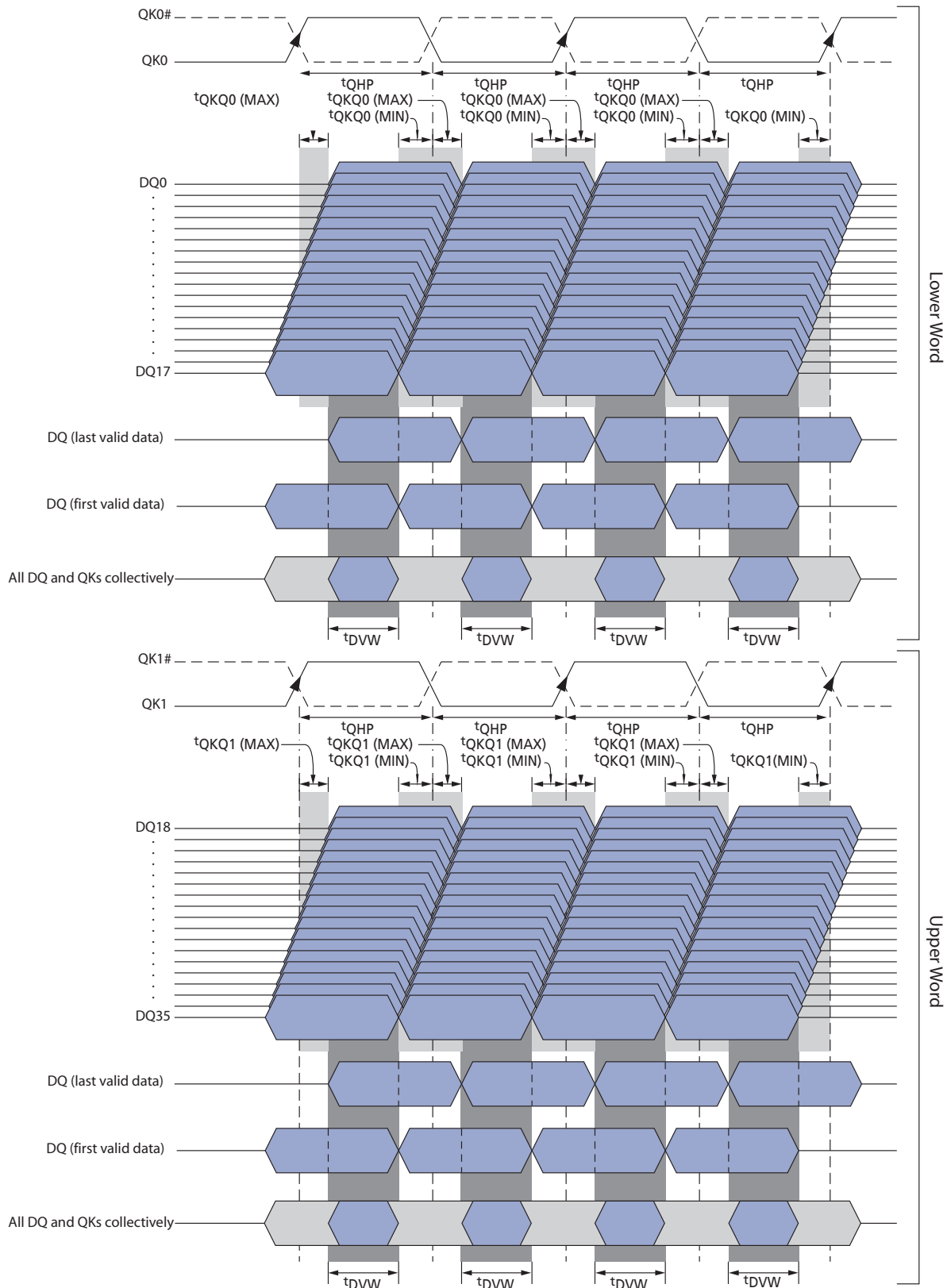
**Table 1: Timing Parameters**

Symbol	-1.8		-2.5/-25E		-3.3		-5		Units
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CK}$ (DLL enabled)	1.875	2.7	2.5	5.7	3.3	5.7	5.0	5.7	ns
$t_{CK}$ (DLL disabled) <sup>1, 2, 3</sup>	1.875	488	2.5	488	3.3	488	5.0	488	ns
$t_{CKH}$	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$
$t_{CKL}$	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$
$t_{CKQK}$ (DLL enabled)	-0.2	0.2	-0.25	0.25	-0.3	0.3	-0.5	0.5	ns
$t_{CKQK}$ (DLL disabled) <sup>3, 4</sup>	0	3.5	0	3.5	0	3.5	0	3.5	ns
$t_{QKQ}$	-0.22	0.22	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns
$t_{QKQ0}, t_{QKQ1}$	-0.12	0.12	-0.2	0.2	-0.25	0.25	-0.3	0.3	ns
$t_{QKVLD}$	-0.22	0.22	-0.3	0.3	-0.35	0.35	-0.4	0.4	ns
$t_{QKH}$	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	$t_{CKH}$
$t_{QKL}$	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	$t_{CKL}$
$t_{QHP}$	Minimum for all speed grades: MIN ( $t_{QKH}, t_{QKH}$ )								ns
$t_{DVW}$	Minimum for all speed grades: $t_{QHP} - (t_{QKQx} [MAX] +  t_{QKQx} [MIN] )$								ns
$t_{CKDK}$	-0.3	0.3	-0.3	0.5	-0.3	1.0	-0.3	1.5	ns
$t_{DS}$	0.17		0.25		0.3		0.4		ns

- Notes:
1. Although running the device at the minimum  $t_{CK}$  with the DLL disabled is possible, closing timing may not be possible at these higher frequencies.
  2.  $t_{CK} \text{ MAX}$  is required to ensure data retention of a single address location.
  3. These AC timing parameters are for reference only and are not tested.
  4.  $t_{CKQK}$  (DLL disabled) is independent of the clock frequency.
  5.  $t_{CKQK}$  (DLL disabled) can vary over its full range due to shifts in process, voltage, and temperature.

Figure 3 on page 4 shows an example of the data valid window and output data timing for the DQ signals to their respective QK clocks on the x36 CIO device. As previously discussed, these parameters do not change whether the DLL is enabled or disabled.

**Figure 3: Data Valid Window and Output Data Timing**



## What Happens in the Dead Band

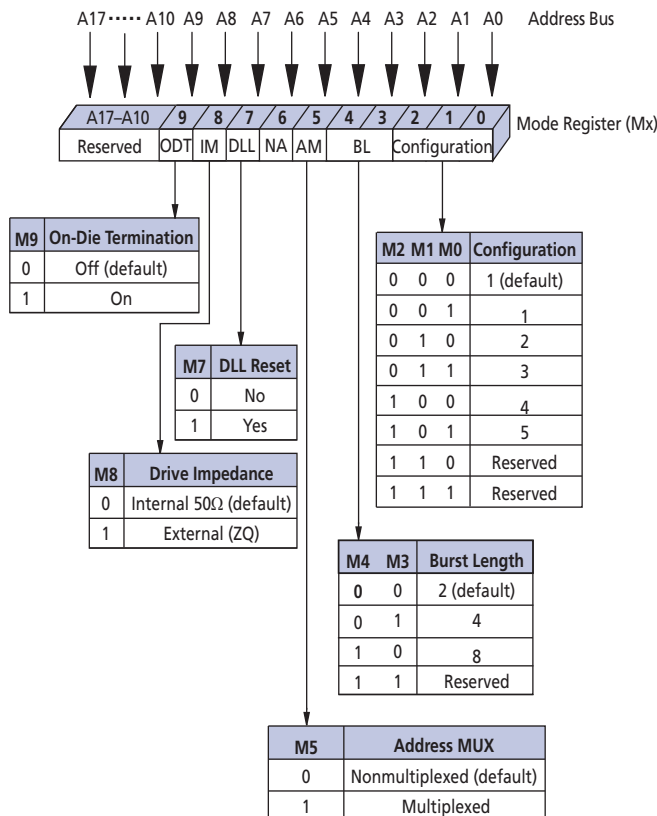
This section provides insight into the device's internal operation and does not constitute guaranteed data timing.

Obviously the RLD RAM II device needs to have some margin designed in; otherwise, Micron could never guarantee any specifications. Here is what happens in the dead band between DLL locked and unlocked: Using the -5 (200 MHz) device as an example, for a clock period of 5–5.7ns, everything runs in accordance with the AC timing specifications. As the clock period increases above 5.7ns, the DLL cannot achieve a lock on the incoming clock, causing the RLD RAM II device to produce larger uncertainty in the output data until a point at which the DLL gain becomes too large to remain stable—potentially causing the RLD RAM II device to miss outputting a data cycle. These undesirable frequencies require the DLL to be disabled in the mode register for operation.

## Disabling the DLL Through the Mode Register

DLL reset is selected with bit A7 of the mode register, as shown in Figure 4. The default setting for this option is LOW, whereby the DLL is disabled. If A7 is set HIGH, 1,024 cycles (5µs at 200 MHz) are needed before a READ command can be issued, enabling the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the <sup>t</sup>CKQK parameter. If the DLL is not enabled through the mode register, these extra cycles are not required.

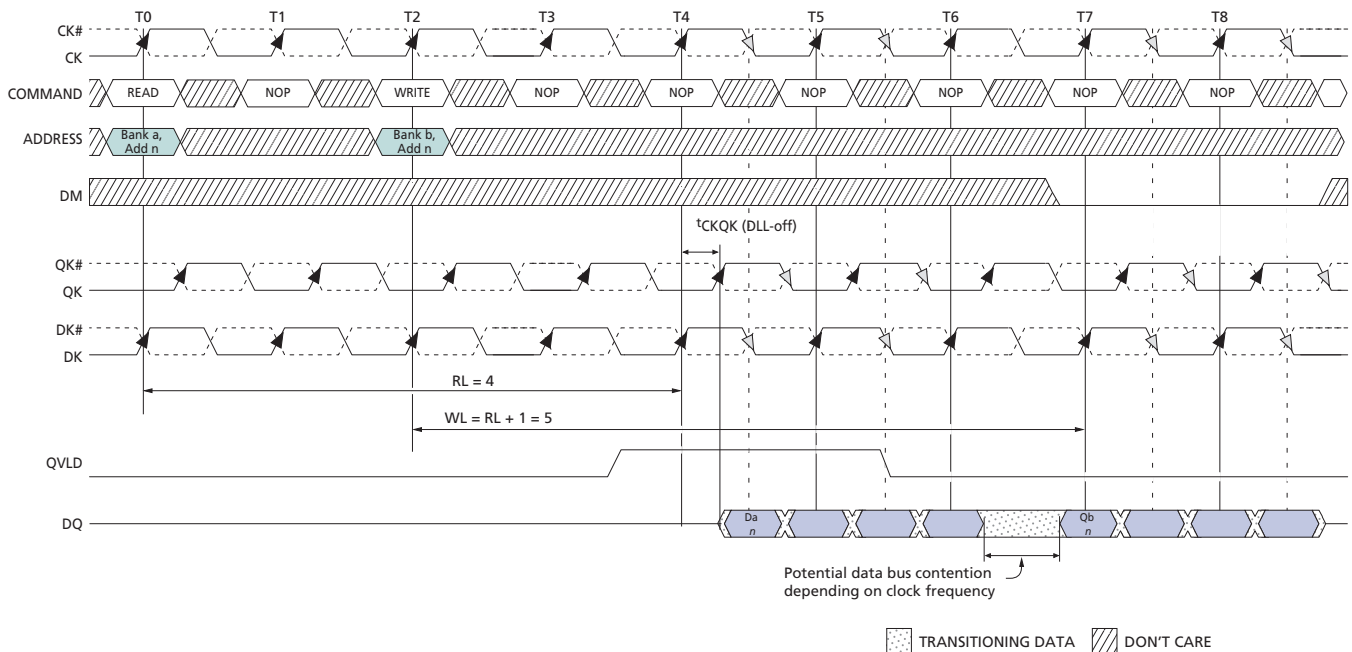
**Figure 4: Mode Register Bit Map**



## Data Bus Transitions

Running the RLD RAM II device with the DLL disabled will have little-to-no effect on the WRITE functionality and timing; however, disabling the DLL does change the output timing of the DQ relative to the input clock. So instead of the DQ transitioning near or at the same time as CK, they are now delayed along with the output QK clocks. The READ latency (RL) remains the same, but the change in the  $t_{CKQK}$  times causes the data to appear up to 3.5ns after the CK transition. At higher frequencies, this can cause a need for an additional clock cycle when going from a READ command to a WRITE command. Figure 5 demonstrates this READ-to-WRITE transition.

**Figure 5: READ-to-WRITE Data Bus Transition**



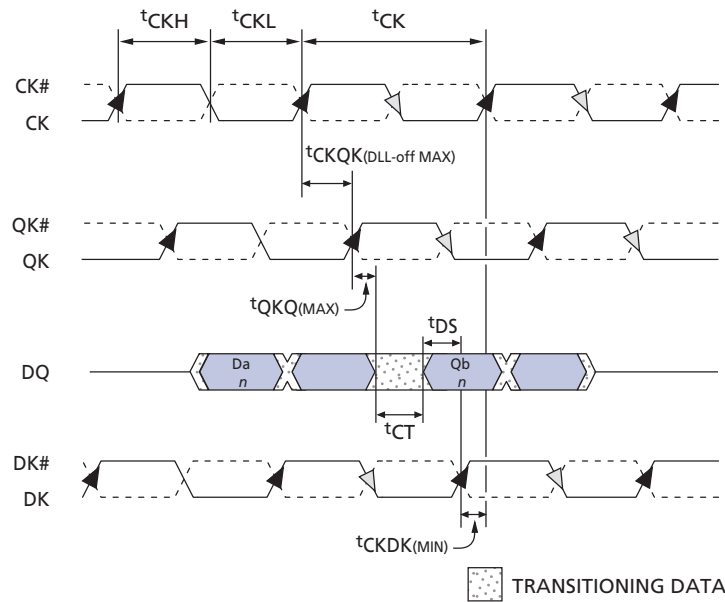
We can calculate the worst-case turnaround time on the data bus with the following equation:

$$t_{CT} = t_{CK} - t_{CKQK} (\text{DLL off [MAX]}) - t_{QKQ} (\text{MAX}) - t_{DS} (\text{MIN}) - |t_{CKDK} (\text{MIN})| \quad (\text{EQ 1})$$

This parameter  $t_{CT}$  can be seen in Figure 6 on page 7. If this value is negative, it is obvious that an extra wait cycle is required on the command and address bus when going from a READ command to a WRITE command. However, this does not take into account other system variables, including signal-flight time, data-hold time at the controller, and output times of the controller. If we assume a clock cycle time of 5ns and worst-case parameters for the -5 speed grade, we see the following:

$$t_{CT} = 5\text{ns} - 3.5\text{ns} - 0.4\text{ns} - 0.4\text{ns} - 0.3\text{ns} \quad (\text{EQ 2})$$

Here we can tell that there is 400ps to turn the data bus around at the RLD RAM II device. Again, this does not take into account a number of additional timing penalties, including the flight time for the READ from the RLD RAM II device to get to the controller and the WRITE from the controller to get to the RLD RAM II device. Including these additional timing penalties will help determine the need for the extra cycle to turn the data bus around.

**Figure 6: READ-to-WRITE Contention at the RLD RAM II Device**


## Conclusion

The RLD RAM II device is equipped with an on-chip DLL to guarantee proper data and data clock generation and alignment. In order to do this, the RLD RAM has a maximum clock cycle time requirement that is needed to ensure stable DLL operation. Violation of the  $t_{CK}(\text{MAX})$  parameter could cause any number of undesirable scenarios, compromising the proper function of the RLD RAM II device. However, as discussed in this document, it is possible to operate the RLD RAM II device while violating the  $t_{CK}(\text{MAX})$  parameter. This requires the disabling of the DLL by way of the mode register. Since the primary reason for including the DLL disable option in the RLD RAM II mode register is to enable system debug and low-frequency testing, only gross functional testing is done in this mode. Full functional testing of the RLD RAM II device is performed with the DLL enabled, to which all timing parameters are established, but no timing parameters are tested with the DLL disabled.



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**This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.**