

Technical Note

Accelerate Design Cycles with Micron® Simulation Models

Introduction

Design engineers face many difficulties when approaching the design of a high-speed memory bus interface. Two of these problems require assistance from the silicon vendor: signal integrity optimization and logic circuit design. Signal integrity problems are a common occurrence due to the high bus speeds in today's systems. Close attention must be paid to high-frequency design rules for layout and impedance matching. The second issue, the increasing complexity of memory devices, has developed because logic that was once relegated to the memory controller has migrated toward the memory device. Controller logic validation requires obtaining behavioral models from the semiconductor manufacturer to use in bus transaction simulations.

Micron recognizes these difficulties and supplies the tools necessary to verify new designs prior to layout. Published data sheets alone are not enough to complete a design. Today's "data sheets" not only provide printed specifications, but also include analog and behavioral simulation models. Making these tools readily available helps streamline the design process, giving customers faster design turnaround and a high degree of confidence in specifying Micron parts.

Which Signal Integrity Model Formats are Provided

Micron currently provides analog signal integrity analysis models for products including SDR/DDR/DDR2 SDRAM, DRAM modules, Mobile DRAM, RLDRAM, CellularRAM™ memory, NAND Flash, and DRAM/NAND Flash multichip packages. Two popular modeling formats are provided for components—Input/Output Buffer Information Specification (IBIS) models and HSpice models. HSpice models are derived from actual device circuit designs. The information contained in the IBIS models is derived from the HSpice models, ensuring that the two model formats provide comparable results. Both models are also checked against laboratory measurements when available. For more information about IBIS-formatted files, see Micron technical note [TN-00-07](#) and visit the official IBIS Web page, www.eigroup.org/ibis/default.htm.

For DRAM module modeling, many popular formats are provided. These include IBIS Electrical Board Description (EBD), Cadence DML, Mentor ICX™, and HyperLynx. Most IBIS EBD models are generated using the Hyperlynx EBD Writer software. Due to the large volume of modules available, models are provided on an as-requested basis.

Support and Distribution of Models

All of Micron's IBIS and HSpice models are updated as new die revisions are qualified or as bugs are discovered. Models are available on Micron's Web site and technical support is available by e-mailing modelsupport@micron.com.

IBIS and HSpice Models for Signal Integrity Analysis

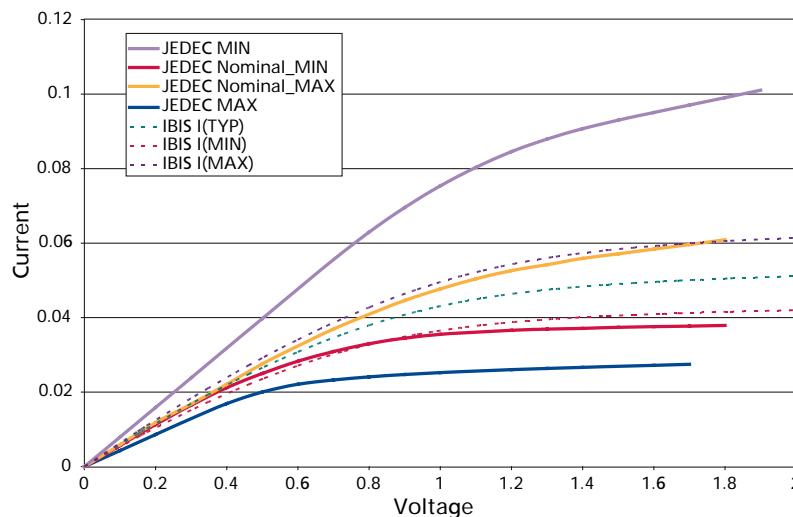
Micron's IBIS and HSpice models are entered into a verification loop before they are released. This process validates proper operation of the IBIS model compared to the HSpice model and compares both models to characterization data from the lab.

The model revision number indicates whether the model has been validated against silicon measurements. A revision 1.x is a pre-silicon model, and indicates that lab measurements have not been used to check the quality of the model. A revision 2.x has had lab measurements compared to the model. Lab measurements can include package parasitics (RLC), input buffer capacitance, input buffer power and ground clamp I-V characteristics, I/O buffer I-V characteristics, and I/O buffer slew rates to standard test loads.

Micron IBIS models also comply with standards set forth by the IBIS Quality Committee. More information on the IBIS Quality Committee checklist can be found at www.vhdl.org/pub/ibis/quality_wip. Additional information found in the IBIS quality header of the IBIS model shows levels of correlation between the IBIS model and lab measurements and/or the HSpice model.

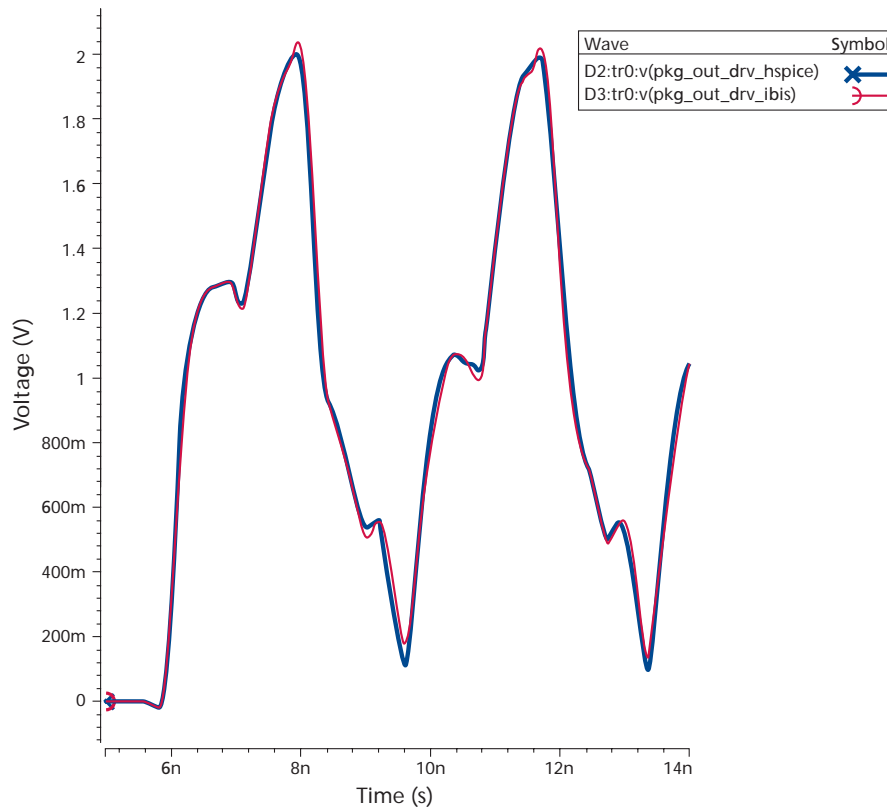
Without lab measurements, models can still be compared to specifications to be sure they fall within certain limits. For instance, many devices must comply with drive strength characteristics set forth by JEDEC. Figure 1 shows an example comparison of a DDR2 DQ buffer's pull-down I-V curve to the JEDEC DDR2 specification. With the availability of lab measurements, several adjustments can be made to the HSpice models to more closely match real device characteristics. Note that lab measurements typically cover voltage and temperature variation of the device, but may not fully cover all process variation found in devices manufactured over time and in different manufacturing facilities. For this reason, adjustments to models are made to match lab measurements while still showing wider variation to account for unmeasured process variation. Buffer capacitance is typically adjusted to a tighter range than indicated by the input capacitance specification found in the data sheet. Diode resistance can be adjusted to match the power and ground clamp diode I-V characteristics. I/O buffer drive strength characteristics may be adjusted through changes to internal model resistance and/or drive strength trimming codes found in many devices. I/O buffer slew rates can be adjusted through pre-driver circuitry slew rate controls.

Figure 1: Comparison of DDR2 Device Pull-Down



Once HSpice models for buffers are adjusted to a specific level of quality, the IBIS model validation process begins. The IBIS model and HSpice model buffers are driven into the same test loads using HSpice as the simulation platform. The waveform results are overlaid and checked to see how well they match. Figure 2 shows an example of an IBIS versus HSpice model simulation. The test load is varied to exercise the IBIS model over a sufficient range. This gives a better indication of how the IBIS model reacts to positive and negative overshoot for inputs and how accurately it behaves when driving transmission lines and varied loads. If there are discrepancies between the IBIS model behavior and the SPICE results, each discrepancy is evaluated to determine which part of the IBIS model caused the inconsistency. Unresolved differences are noted in the IBIS model.

Figure 2: IBIS Model vs. HSpice (No ODT) Nominal Process, Voltage, and Temperature



IBIS and HSpice Model Limitations

There are limitations with all modeling formats, and it is important that customers be aware of these. HSpice models typically provide the most flexibility, enabling the user to simulate all combinations of process, voltage, temperature (PVT) variations. However, many new devices adjust the I/O buffer output impedance using a series of codes that turn on or off sets of transistors in the driver. These codes may be fixed in the device or they may change dynamically in response to changes in voltage or temperature during device operation. This second option is seen in DDR3 devices. The HSpice models are set up to run with specific combinations of PVT, such as slow process, low voltage, and high temperature. Therefore, specific codes are set up in the models for these corner conditions. If the user needs to use different combinations of PVT than given in the supplied model, they will need to contact Micron for code updates.

IBIS models have significantly different limitations than HSpice models. IBIS models are extracted from HSpice models at specific PVT corner conditions. The user is limited to the PVT conditions set up in the model; if different conditions are required, a request for a new model will need to be made. Also, the length in time of voltage versus time (V-t) curves that characterize I/O buffers determines the maximum operating speed of the model. For example, if the length of V-t curves for a buffer is 1.875ns, this dictates a maximum operating speed of 533 Mb/s for a DDR2 device. For this reason, there may be different IBIS models for devices at higher operating frequencies, where only devices with fast transistor characteristics make the fastest speed grade bin. Other limitations with IBIS include the ability to model package and die high-frequency loss characteristics. Micron is committed to providing high-quality models and works closely with the IBIS Open Forum to improve model quality and to model the latest technologies.

DRAM module models can also be problematic. Current model formats such as IBIS EBD do not provide methods for modeling crosstalk between traces. There are also problems with EDA software that does not fully support all IBIS keywords, limiting the ability to describe termination schemes on modules. Micron provides models in IBIS EBD, Mentor ICX, Cadence DML, and HyperLynx formats to combat this issue.

Behavioral Models for Circuit Design Verification

Validation of Verilog Models

Behavioral models provided by Micron are written in the Verilog synthesis language.

The verification process for Micron's behavioral models extends to the operation described in the data sheet specifications. Micron manufactures devices that follow specifications established by the JEDEC standards committee; therefore, all product data sheets describe only the industry-accepted operating modes for the device. Operating modes that are particular to Micron's design are not described in the data sheets. Similarly, and as a service to customers who may use competitors' designs, Micron's behavioral models are not written to emulate any operating modes outside data sheet specifications.

After the preliminary code describing the design behavior is written, test vectors are developed that test the timing checks and logic of the behavioral model. The test bench is written to test for race conditions, invalid logic implementation, and proper operation of the output logic. When minimum and maximum times are given for a timing parameter, the model is written so that unknown states are placed on the bus for times between the minimum time the bus may not be available and the time a known state will be on the bus. This way, a circuit is verified to the worst-case conditions available from the device.

The test bench is also written to provide input variables through a text file. The test bench then applies the inputs to the behavioral model, and the output is verified against data sheet specifications. Conditions of operation are varied so all possible combinations of state transitions can be simulated to verify proper operation, and all example conditions presented in the data sheet are tested and verified. Then, all timing violation checks are tested and verified to the timing parameters given in the data sheet.

Using Behavioral Models Provided by Micron

Traditional design verification techniques require a set of test vectors that represent all possible input combinations developed by the design engineer. These test vectors are then applied in design simulations, and the output from the simulations is compared to

the design specifications. This is the method Micron uses to verify behavioral model designs. However, when a complex design such as an ASIC is developed using the Verilog language, these techniques become prone to errors because they rely on interpretations between simulation output and expected output. In addition, any functionality missed by the test vectors will be missed by the simulation.

Formal design validation tools are being developed that compare two levels of a design description to verify correct logic at the gate level. These tools can validate a behavioral description of a design against a register transfer level (RTL) description before synthesis is completed. The behavioral models provided by Micron assist in developing an accurate behavioral model. Without a behavioral model of the memory device, validation of the design behavioral model interfacing to the memory device becomes an exercise in validating the design behavior against memory device data sheet specifications. Without the memory device behavioral model, design errors can be made at the behavioral level, thus propagating design errors to the RTL level. This is why a behavioral model of the memory device can be crucial to a successful design.

Using a behavioral model to verify a design depends on the experience the hardware designer has had with a particular type of device and the complexity of the device. Often, logic interfaces to memory devices can be designed without the aid of a behavioral model because data sheet specifications provide enough information to complete the design. However, as memory devices perform more complex functions, it becomes extremely difficult, and even impossible, to verify a design prior to hardware implementation without the aid of a behavioral model. Because behavioral models are required to complete simulation verification of a design, Micron has developed behavioral models for SDR/DDR/DDR2 SDRAM, Mobile DRAM, CellularRAM, NAND Flash, and DRAM/NAND Flash multichip packages to help expedite controller designs. Future model development will depend on device complexity and customer demand.

Summary

Micron has assumed an active role in helping customers complete new designs faster and with a greater degree of confidence. Increasing bus frequencies demand that analog I/O models be available to complete signal integrity analysis of a design. As more complex functions are incorporated into the memory device, behavioral models become increasingly important in completing simulations for circuit verification. Having recognized this, Micron will continue improving customer service by providing software model support.



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Revision History

Rev. C	10/06
<ul style="list-style-type: none">• Updated template• Updated text and graphics throughout	
Rev. B	9/99
Rev. A	1/97
<ul style="list-style-type: none">• Initial release	