

# TECHNICAL NOTE

# CALCULATING MEMORY SYSTEM POWER FOR DDR

## INTRODUCTION

Today's system designer is concerned about the power used by the main memory in the system. Whether it is calculating battery life for a portable application, planning cooling for a "pizza box" desktop, or determining the power supply for a server, an accurate power budget for the memory is essential. Unfortunately, the data sheets do not always make it easy to determine how much power is used by each device in a specific application.

DDR SDRAM allows for lower power consumption than other memory solutions. This application note explains how power is used by DDR SDRAM and provides some basic tools to help calculate the system power that is consumed by the DRAM. These tools can

be adapted to fit a wide range of applications and even help identify simple methods for modifying a system to use less power without significantly affecting the system's performance. After all, a high-performance system will disappoint if it overheats or the battery life fails to meet end users' expectations.

While this technical note is targeted at tools and techniques to calculate system power, actual examples are also provided. An example data sheet is given in Appendix A and examples are provided in Appendix B. Values provided in data sheets may differ from vendor to vendor, over time, but the concepts behind calculating power for both single and double data rate SDRAMs are the same. For the purposes of discussion, this technical note focuses on DDR SDRAM.

## TABLE OF CONTENTS

DRAM Operation .....	2
DRAM Power Calculations .....	3
CKE Operation .....	3
Activate Power .....	3
Write Power .....	5
Read Power .....	6
Refresh Power .....	8
Power Derating .....	8
Voltage Supply Scaling .....	8
Frequency Scaling .....	8
Calculating Total System Power .....	9
Summary .....	10
<b>Appendix A: Data Sheet Assumptions</b> .....	11
<b>Appendix B: Examples</b> .....	12
DDR200 Moderate Usage Example .....	12
DDR266 High-Stress Workload Example .....	14
<b>Appendix C: Adapting to Calculate SDRAM System Power</b> .....	15



## DRAM POWER CALCULATIONS

For this technical note, the  $I_{DD}$  values are shown in Appendix A. This is an extraction from a 128Mb DDR SDRAM data sheet. Other values may be substituted if the device data sheet is different. It is the engineer's responsibility to verify all data sheet parameters before using this information.

## CKE OPERATION

As stated previously, CKE (clock enable) is the master on-off switch for the DRAM. When CKE is LOW, all inputs, including clocks, are disabled. This is the lowest power state in which the device may operate. This power is specified in the data sheet at  $I_{DD2P}$  if all the banks are precharged, and  $I_{DD3P}$  if any bank is active.

CKE must be taken HIGH to read or write data to the DDR SDRAM. Upon CKE going HIGH, the clock signals start propagating through the DDR SDRAM and the device is prepared to start receiving commands. This activity within the DRAM increases the power consumption and is specified in the data sheet at  $I_{DD2F}$  if all the banks are precharged and  $I_{DD3N}$  if any bank is active.

Figure 2 shows the typical current usage on a DDR SDRAM device when CKE is transitioned. When CKE is HIGH, the device draws approximately 40mA of current; when CKE goes LOW, it drops to 5mA..

**Figure 2: Effects of CKE**

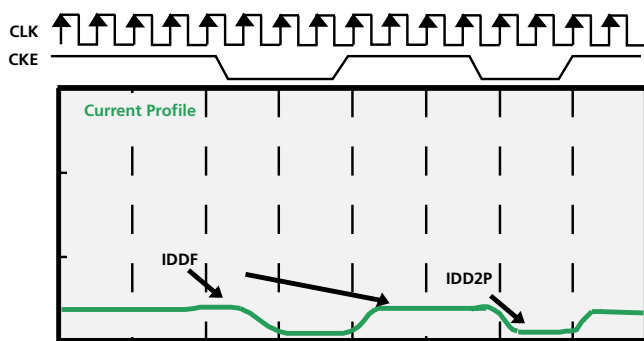


Figure 2 assumes the device is in precharge state. Thus when CKE is HIGH, the DDR SDRAM uses  $I_{DD2F}$  current; and when CKE is LOW, it uses  $I_{DD2P}$  current. Similarly, if the device is in active state, it consumes  $I_{DD3P}$  current in power-down state (CKE = LOW) and  $I_{DD3N}$  current in standby (CKE = HIGH).

The power consumed by the DDR SDRAM is easily calculated by multiplying the  $I_{DD}$  values by the voltage applied to the device  $V_{DD}$ .

### Equation 1a

$$p(\text{PRE\_PDN}) = I_{DD2P} * V_{DD}$$

### Equation 1b

$$p(\text{PRE\_STBY}) = I_{DD2F} * V_{DD}$$

### Equation 1c

$$p(\text{ACT\_PDN}) = I_{DD3P} * V_{DD}$$

### Equation 1d

$$p(\text{ACT\_STBY}) = I_{DD3N} * V_{DD}$$

Note that the data sheet values for all  $I_{DD}$  values are taken at worst-case  $V_{DD}$ , which for the DDR SDRAM is 2.7V. The equations are solved as follows:

### Equation 2a

$$p(\text{PRE\_PDN}) = 3\text{mA} * 2.7\text{V}$$

$$p(\text{PRE\_PDN}) = 8\text{mW}$$

### Equation 2b

$$p(\text{PRE\_STBY}) = 45\text{mA} * 2.7\text{V}$$

$$p(\text{PRE\_STBY}) = 122\text{mW}$$

### Equation 2c

$$p(\text{ACT\_PDN}) = 18\text{mA} * 2.7\text{V}$$

$$p(\text{ACT\_PDN}) = 49\text{mW}$$

### Equation 2d

$$p(\text{ACT\_STBY}) = 45\text{mA} * 2.7\text{V}$$

$$p(\text{ACT\_STBY}) = 122\text{mW}$$

## ACTIVATE POWER

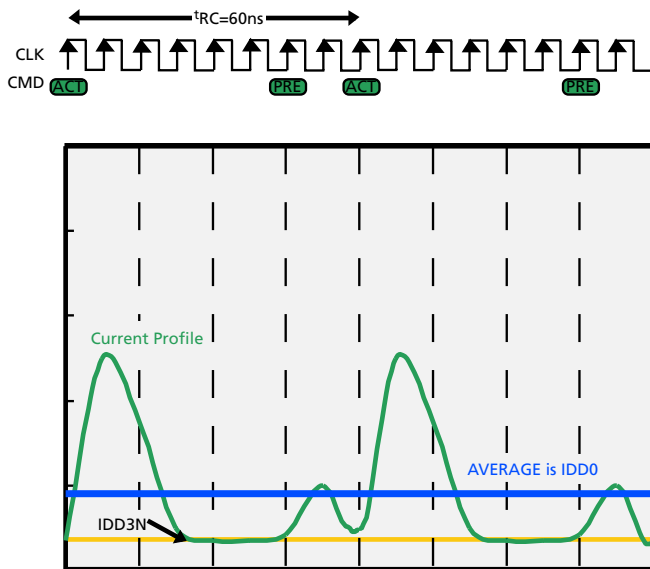
To be useful, a DDR SDRAM must read and write data. In order to complete this task, a row must first be selected using an ACTIVATE (ACT) command, along with a bank and row address.

For every ACT command, there is a corresponding PRECHARGE (PRE) command. Where the ACT command opens a row, the PRE closes the row. While other commands may be present, the ACT and PRE commands are always paired together.

As shown in Figure 3, the ACT and PRE commands cause significant activity in the DRAM. The current required for this activity is determined using the  $I_{DD0}$  specification in the data sheet. The time between successive ACT commands in the same bank is specified as the minimum  $t_{RC}$ .

Figure 3 shows a typical current profile for  $I_{DD0}$ . After the ACT command, a large amount of current is used while the command/address is decoded and the data from the DRAM array is transferred to the sense amplifiers. Once this is complete, the DRAM is maintained in an active state and draws  $I_{DD3N}$  until a PRE command is issued. The PRE command restores the data from the sense amplifiers into the memory array and resets the bank for the next ACT command. Once this is complete, the device is returned to precharge state. This cycle is then repeated at  $t_{RC}$  intervals between ACT commands.

**Figure 3:  $I_{DD0}$  Current Profile**



The  $I_{DD0}$  value specified in the data sheet is the average current required for device operation. In Figure 3, this is represented by the blue line. During this time, CKE is held HIGH so the device is always drawing a base amount of current ( $I_{DD3N}$ ). [This current was calculated as  $p(\text{ACT\_STBY})$  in Equation 2d.] Therefore, to calculate the power consumed by the ACT-PRE pair,  $p(\text{ACT})$ ,  $I_{DD3N}$  must be subtracted from  $I_{DD0}$  prior to multiplying by the maximum  $V_{DD}$ .

**Equation 3**

$$p(\text{ACT}) = [I_{DD0} - I_{DD3N}] * V_{DD}$$

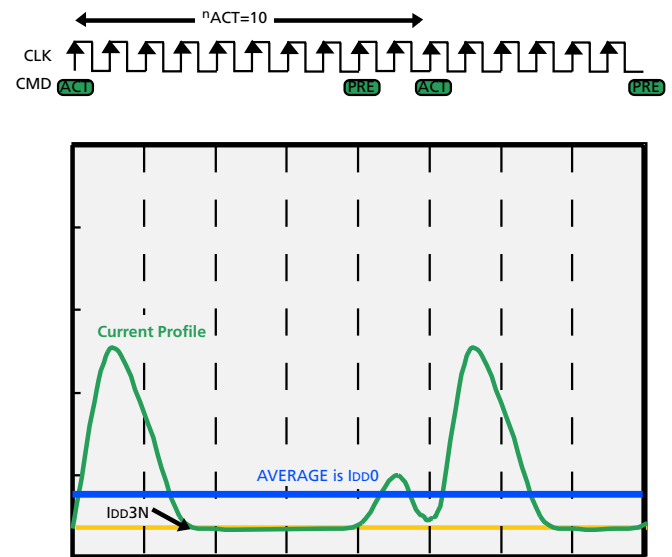
$$p(\text{ACT}) = [105\text{mA} - 45\text{mA}] * 2.7\text{V}$$

$$p(\text{ACT}) = 162\text{mW}$$

This equation is correct if the DRAM is only used at minimum  $t_{RC}$  cycle time. However, it is unlikely that most systems operate in this manner. Fortunately, it is easy to scale the ACT current for other modes of operation. We will apply this to two examples: when ACT-ACT cycle time is greater than  $t_{RC}$ , and when the device is in bank interleave mode.

Refer to Figure 4 for an example where the ACT-ACT cycle time is greater than the specified  $t_{RC} = 60\text{ns}$ . The  $t_{RC}$  is stretched to 10 clock cycles. A new parameter,  $n_{\text{ACT}}$ , is used to signify the number of clock cycles between ACT cycles.

**Figure 4: ACT-ACT Current With  $t_{RC} = 10 t_{CK}$**



The  $I_{DD0}$  value can easily be scaled as a ratio of the actual ACT-ACT duration to the data sheet conditions. The assumption is that the clock is operating at 133 MHz, so  $t_{CK} = 7.5\text{ns}$ . Notice that  $I_{DD3N}$  is not scaled. Therefore, it must be subtracted from the ratio. The calculations are as follows:

**Equation 4**

$$p(\text{ACT}) = (I_{DD0} - I_{DD3N}) * \frac{t_{RC}(\text{spec}) * V_{DD}}{n_{\text{ACT}} * t_{CK}}$$

$$p(\text{ACT}) = (105\text{mA} - 45\text{mA}) * \frac{60\text{ns}}{10\text{CK} * 7.5\text{ns/CK}} * 2.7\text{V}$$

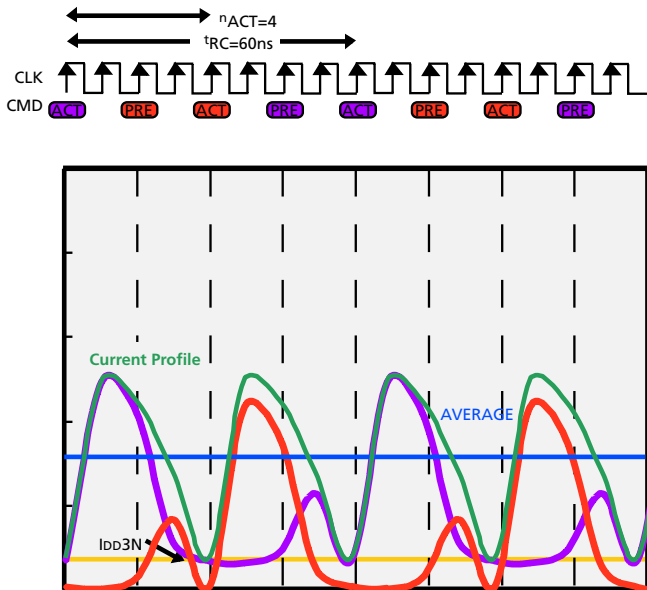
$$p(\text{ACT}) = 130\text{mW}$$

Therefore, by changing the ACT-ACT time from 8 tCK to 10 tCK, the activation power, p(ACT), drops from 162mW to 130mW. Note, this power is only the activation power and does not include the background power contributed by I<sub>DD3N</sub>.

Because there are multiple banks on the DDR SDRAM, it is possible to have several banks open at one time. Therefore, it is also possible to have ACT commands closer together than t<sub>RC</sub>. Figure 5 shows an example where two banks are interleaved. Each bank has t<sub>RC</sub> = 8 tCK. Therefore, the average time between ACT cycles is n<sub>ACT</sub> = 4

The purple current profile is for the first bank activated and includes the I<sub>DD3N</sub> component. This is only included once on the device even if other banks are open. Therefore, the red current profile, representing the second bank activated, is offset by I<sub>DD3N</sub>. The green curve represents the summation of the two banks.

**Figure 5: ACT-ACT Separation of 4 tCK**



The calculation to determine the power consumption for the activation power is the same as before.

**Equation 5**

$$p(\text{ACT}) = (I_{\text{DD0}} - I_{\text{DD3N}}) * \frac{t_{\text{RC}}(\text{spec})}{n_{\text{ACT}} * t_{\text{CK}}} * V_{\text{DD}}$$

$$p(\text{ACT}) = (105\text{mA} - 45\text{mA}) * \frac{60\text{ns}}{4\text{CK} * 7.5\text{ns}/\text{CK}} * 2.7\text{V}$$

$$p(\text{ACT}) = 324\text{mW}$$

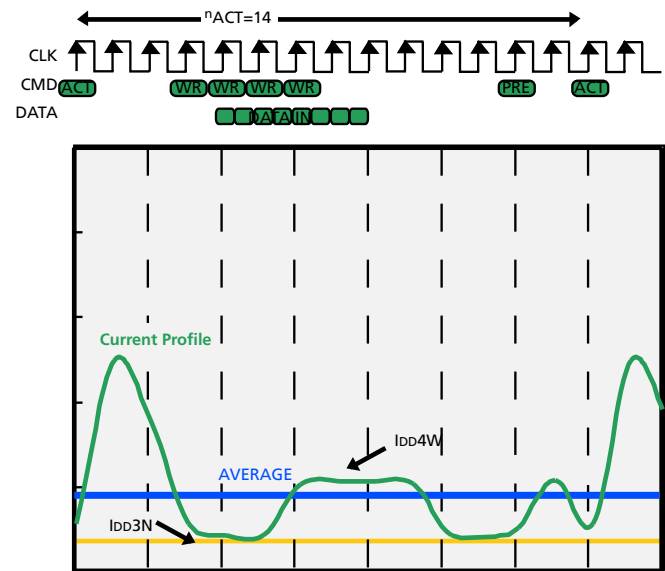
The p(ACT) for two interleaved banks increases from 162mW to 324mW. This is intuitive because twice the amount of ACT and PRE power is consumed when operating two banks compared to one bank.

With this basic equation, the ACT-PRE power can be calculated over any usage condition, from four interleaved banks to one bank that is seldom opened.

**WRITE POWER**

Once a bank is open, the data can either be read from or written to the DDR SDRAM. The two cases are similar and the write case will be calculated first. Figure 6 shows an example of a WRITE cycle.

**Figure 6: WRITE Cycle**



As with the ACT-PRE command sequence, the DDR SDRAM uses a peak of power after the ACT command and a smaller amount of current after the PRE command. If a WRITE does not occur, the current consumption remains at I<sub>DD3N</sub> between these two peaks of current.

However, when several WRITES are added, the consumption of current associated with the WRITE is I<sub>DD4W</sub>. I<sub>DD4W</sub> is typically specified as continuous WRITES. The amount of additional power required for the WRITE shown in Figure 6 is calculated as follows:

**Equation 6**

$$p(\text{WR}) = (I_{\text{DD4W}} - I_{\text{DD3N}}) * \frac{\text{num of WR cycles}}{n_{\text{ACT}}} * V_{\text{DD}}$$

$$p(\text{WR}) = (110\text{mA} - 45\text{mA}) * \frac{4\text{CK}}{14\text{CK}} * 2.7\text{V}$$

$$p(\text{WR}) = 50\text{mW}$$

First, the amount of additional current required for the WRITE is calculated by subtracting the background current from the write current ( $I_{DD4W} - I_{DD3N}$ ). This current is only used during the WRITE cycles so it is a ratio of the number of WRITE cycles over the total cycles,  $t_{ACT}$ . Finally, this is multiplied by  $V_{DD}$  to calculate the device power.

It is now also possible to calculate the total device power, which includes the write power, the ACT power, and the active standby power.

First, the  $p(ACT)$  is calculated by substituting Figure 6 values into Equation 4:

### Equation 7

$$p(ACT) = (I_{DD0} - I_{DD3N}) \frac{t_{RC(spec)} * V_{DD}}{t_{ACT} * t_{CK}}$$

$$p(ACT) = (105mA - 45mA) * \frac{60ns}{14CK * 7.5ns/CK} * 2.7V$$

$$p(ACT) = 93mW$$

$p(ACT\_STBY)$  was calculated previously in Equation 2d, so the three power components can now be added together.

### Equation 8

$$p(TOT) = p(ACT) + p(WR) + p(ACT\_STBY)$$

$$p(TOT) = 93mW + 50mW + 122mW$$

$$p(TOT) = 265mW$$

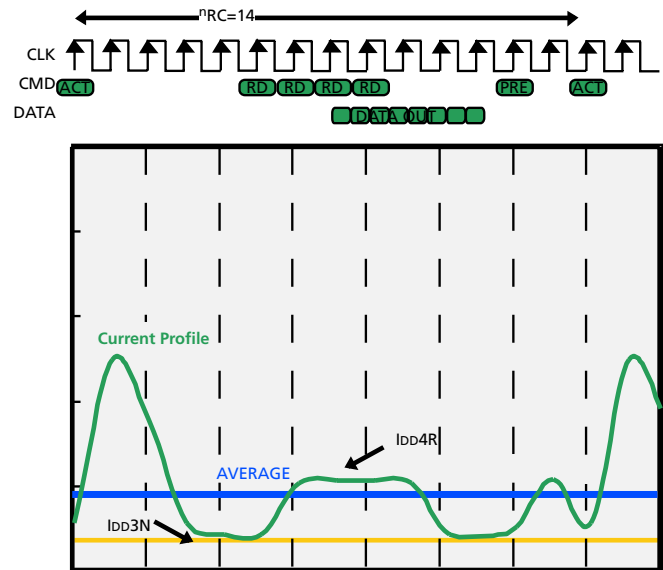
Therefore, to write eight words (four clocks) of data to the DDR SDRAM with an average cycle time of 14 clocks requires 265mW of power.

One thing to note is the test conditions for  $I_{DD4W}$ . As noted in Appendix A,  $I_{DD4W}$  is tested with  $BL = 2$ . Often DDR SDRAMs are operated with burst lengths other than two. If this occurs, the DDR SDRAM generates the additional addresses for the column locations for the subsequent bits in the data burst. The power consumed is still approximated by counting how many clocks of data-in are used for the WRITE. Therefore, if a WRITE using  $BL = 8$  is completed, it would be the equivalent power of four WRITES with  $BL = 2$  (four clock cycles).

## READ POWER

The power to read data is similar to that of writing data. The data sheet specifies the read current as  $I_{DD4R}$ . A current profile of a READ is shown in Figure 7. In this example, a row is opened with an ACT command and four cycles later, a burst of four READs (two clocks) is started to columns in that row. After the READs are complete, the row is closed with a PRECHARGE command and the sequence is restarted.

**Figure 7: Read Current Profile**



The read current profile looks very similar to the write current profile. The average current is calculated exactly the same as the write case except  $I_{DD4R}$  is substituted for  $I_{DD4W}$ .

### Equation 9

$$p(RD) = (I_{DD4R} - I_{DD3N}) * \frac{\text{num of RD cycles} * V_{DD}}{t_{ACT}}$$

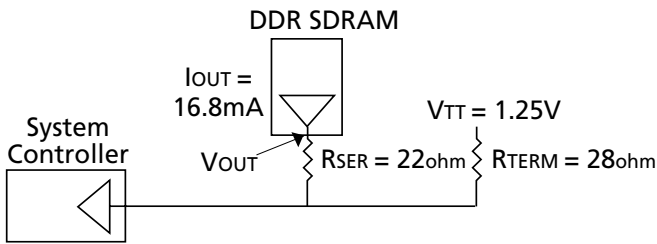
$$p(RD) = (110mA - 45mA) * \frac{4CK}{14CK} * 2.7V$$

$$p(RD) = 50mW$$

However, this isn't the complete answer for the amount of power consumed during a READ. The note attached to  $I_{DD4R}$  in Appendix A specifies  $I_{DD4R}$  with  $I_{OUT} = 0mA$ . Thus, to get the full current consumption for the READ case, the value of  $I_{OUT}$  must be calculated.

This calculation will be different for each system depending on the termination scheme used. A typical DDR SDRAM system is shown in Figure 8. During READs, each output on the DDR SDRAM sinks/supplies 16.8mA. The termination consists of a 22 ohm series (typically on the modules) and a 28 ohm series resistor to  $V_{TT} - 1.25V$  (typically on the motherboard).

**Figure 8: Typical System DQ Termination**



The worst-case output power is the DC case of driving a one or zero over multiple clock cycles. This is most easily calculated by determining  $V_{OUT}$  first.

**Equation 10**

$$V_{OUT} = 1.25V - I_{OUT} * (R_{SER} + R_{TERM})$$

$$V_{OUT} = 1.25V - 16.8mA * (22\text{ ohm} + 28\text{ ohm})$$

$$V_{OUT} = 0.41V$$

The power for the DQs is calculated as shown below. First the power per output driver,  $p(\text{perDQ})$ , is calculated as  $V_{OUT} * I_{OUT}$ . This is multiplied by the number of DQ and DQS pins. This example is assumed to be a x8 device, so there are eight DQs and one DQS. The power includes the power for the DQS signal, which is also driving anytime data is being output. Finally, the total is multiplied by the ratio of RD cycles versus total cycles (same as for write power).

**Equation 11**

$$p(\text{perDQ}) = V_{OUT} * I_{out}$$

$$p(\text{perDQ}) = 0.41V * 16.8mA$$

$$p(\text{perDQ}) = 6.88mW$$

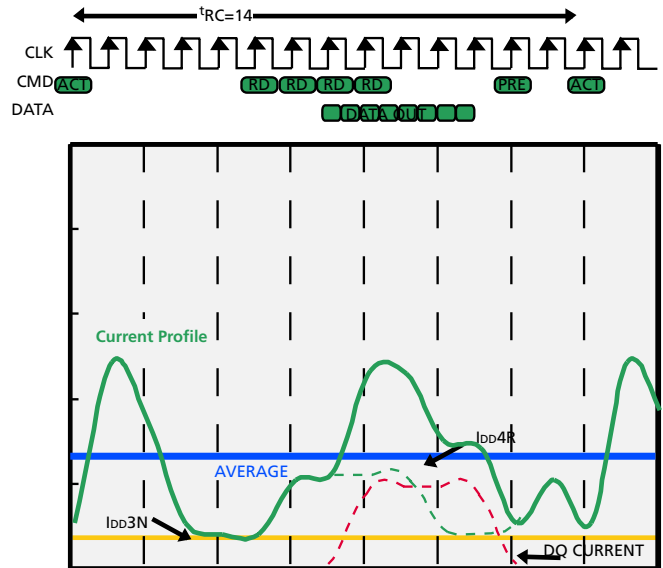
$$p(DQ) = p(\text{perDQ}) * (\text{num\_of\_DQ} + \text{num\_of\_DQS}) * \frac{\text{num of RD cycles}}{n_{ACT}}$$

$$p(DQ) = 6.88mW * (8 + 1) * \frac{4CK}{14CK}$$

$$p(DQ) = 17mW$$

This output power is consumed while the outputs are actually driving data. Figure 9 shows the current profile if the DQ power is included in a READ cycle. (The dashed green line is the  $I_{DD4R}$  line.) To drive the outputs, an additional DQ current is required (and represented by the dashed red line). Adding these two lines together provides the total current profile (solid green line).

**Figure 9: Read Current with I/O Power Included**



To calculate the total power for this DDR SDRAM READ operation, first determine the ACTIVATE power using Equation 4:

**Equation 12**

$$p(ACT) = (I_{DD0} - I_{DD3N}) \frac{t_{RC}(\text{spec}) * V_{DD}}{n_{ACT} * t_{CK}}$$

$$p(ACT) = (105mA - 45mA) * \frac{60ns}{14CK * 7.5ns/CK} * 2.7V$$

$$p(ACT) = 93mW$$

Next, the read power is calculated. Note the I/O power is added to the DDR SDRAM read power and then the ratio of the number of READ cycles is taken.

Once the subcomponents of the power are determined, they are simply added together as shown previously. ( $p(ACT)$  is from Equation 12;  $p(RD)$  is from Equation 9;  $p(DQ)$  is from Equation 11; and  $p(ACT\_STBY)$  is from Equation 2d.)

**Equation 13**

$$p(TOT) = p(ACT) + p(RD) + p(DQ) + p(ACT\_STBY)$$

$$p(TOT) = 93mW + 50mW + 17mW + 122mW$$

$$p(TOT) = 282mW$$

READs, like WRITEs, can be completed with various burst lengths. Although the data sheet is specified with BL = 2, this can be applied to any other burst length. As in the write condition, as long as the actual number of clocks are used for the power ratio, the resulting calculation will approximate the power independent of burst length.

## REFRESH POWER

One final power component must be calculated for an SDRAM to retain data integrity in the system. The memory cells of a DDR SDRAM store the data information in small capacitors that lose their charge over time and must be recharged. This process is called refresh. The refresh operation is normally distributed evenly over time. This is specified assuming the device is in precharge power-down at all times except when the actual REFRESH commands are executed. Thus, the average power for the refresh functionality is:

### Equation 14

$$\begin{aligned} p(\text{REF}) &= (I_{\text{DD5}} - I_{\text{DD2P}}) * V_{\text{DD}} \\ p(\text{REF}) &= (5\text{mA} - 3\text{mA}) * 2.7\text{V} \\ p(\text{REF}) &= 5\text{mw} \end{aligned}$$

## POWER DERATING

Thus far, the power calculations have assumed the system was operating at the worst-case  $V_{\text{CC}}$ . They also assumed the clock frequency in the system is the same as the frequency defined in the data sheet. The resulting power is denoted as  $p(\text{spec cond})$ . However, most systems operate at different clock frequencies or operating voltages than the ones defined in the data sheet. Each of the power components must be derated to the actual system conditions. The resulting power is noted at  $P(\text{use cond})$ . (Note: Powers designated with a “p” are worst-case  $V_{\text{CC}}$  and data sheet clock frequency, while “P” denotes the derated power for system  $V_{\text{CC}}$  and clock frequency.) The following section explains how to derate each of the power components to the actual system operation.

## VOLTAGE SUPPLY SCALING

All power calculations thus far have been calculated at maximum specified  $V_{\text{DD}}$ . However, few systems operate at such conditions. Systems often operate closer to a nominal  $V_{\text{DD}}$ . Most of the power components scale as  $V_{\text{DD}}$  changes. The only power parameter that does not scale with  $V_{\text{DD}}$  is  $p(\text{DQ})$ .

Power is related to the square of the voltage supply. Thus, to scale power to a different supply voltage:

### Equation 15

$$P(\text{use } V_{\text{DD}}) = p(\text{spec } V_{\text{DD}}) * \frac{(\text{use } V_{\text{DD}})^2}{(\text{max spec } V_{\text{DD}})^2}$$

## FREQUENCY SCALING

Similarly, many of the power components are dependent on the clock frequency at which the device is operating. These include  $p(\text{ACT\_STBY})$  (Equation 1d);  $p(\text{IDLE\_STBY})$  (Equation 1b);  $p(\text{WR})$ ;  $p(\text{RD})$ ; and  $p(\text{DQ})$ .

Other powers, such as  $P(\text{PRE\_PDN})$ ,  $P(\text{ACT\_PDN})$ , are not dependent on operating clock frequency because the clock is disabled during power-down mode.  $P(\text{ACT})$  is also not clock frequency dependent as it is only dependent on the interval between ACT commands. Similarly,  $P(\text{REF})$  does not scale with clock frequency.

For the powers that are operating frequency dependent, the power can be scaled for actual operating frequency:

### Equation 16

$$P(\text{use freq}) = p(\text{spec freq}) * \frac{(\text{use freq})}{(\text{spec freq})}$$

The use\_freq is the actual clock frequency that the device is operating at in the system. The spec\_freq is the clock frequency that the device was tested at during the I<sub>DD</sub> tests. This information is provided in the test condition notes in the data sheet. The notes describe that the device is tested at the minimum clock rate for a specific CAS latency. This value is specified under the t<sub>CK</sub> parameter.

**Equation 17**

$$\begin{aligned}
 P(\text{PRE\_PDN}) &= p(\text{PRE\_PDN}) * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{ACT\_PDN}) &= p(\text{ACT\_PDN}) * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{PRE\_STBY}) &= p(\text{PRE\_STBY}) * \frac{(\text{use freq})}{(\text{spec freq})} * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{ACT\_STBY}) &= p(\text{ACT\_STBY}) * \frac{(\text{use freq})}{(\text{spec freq})} * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{ACT}) &= p(\text{ACT}) * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{WR}) &= p(\text{WR}) * \frac{(\text{use freq})}{(\text{spec freq})} * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{RD}) &= p(\text{RD}) * \frac{(\text{use freq})}{(\text{spec freq})} * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2} \\
 P(\text{DQ}) &= p(\text{DQ}) * \frac{(\text{use freq})}{(\text{spec freq})} \\
 P(\text{REF}) &= p(\text{REF}) * \frac{(\text{use } V_{DD})^2}{(\text{max spec } V_{DD})^2}
 \end{aligned}$$

## CALCULATING TOTAL SYSTEM POWER

The tools are now in place to calculate the system power for any usage condition. The last task is putting them all together. To determine the DDR SDRAM operation of a system, the following components are needed for input.

V <sub>DDsys</sub>	System V <sub>DD</sub> that the device is operating. This is typically closer to a nominal value of 2.5V
FREQ <sub>sys</sub>	Frequency at which the system clock to the DDR SDRAM is operating
P(perDQ)	The output power of a single DQ (as calculated earlier).
BNK_PRE%	Percentage of time all banks are precharged
CKE_LO_PRE%	Percent of the banks' PRE time that CKE is LOW
CKE_LO_ACT%	Percent of the ACT time that CKE is LOW
t <sub>ACT</sub>	The average time between ACT commands
RD%	Percentage of CK cycles that output read data
WR%	Percentage of CK cycles that input write data

To determine the system power, each of these parameters are applied to the equations already discussed. First, the standby/power-down currents are ratioed to actual system use. The equations below are modified from Equation 1, which adds the percentages of time the device is precharged and the percentage of time the device is in power-down mode. Note that these numbers cover 100 percent of the total device operating time. During actual device operation (ACTIVATES, READS, WRITES), the device is starting from a base power of p(ACT\_STBY).

**Equation 18**

$$\begin{aligned}
 p(\text{PRE\_PDN}) &= I_{DD2P} * V_{DD} * \text{BNK\_PRE\%} * (\text{CKE\_LO\_PRE\%}) \\
 p(\text{PRE\_STBY}) &= I_{DD2F} * V_{DD} * \text{BNK\_PRE\%} * \text{CKE\_LO\_PRE\%} \\
 p(\text{ACT\_PDN}) &= I_{DD3P} * V_{DD} * (1 - \text{BNK\_PRE\%}) * (1 - \text{CKE\_LO\_ACT\%}) \\
 p(\text{ACT\_STBY}) &= I_{DD3N} * V_{DD} * (1 - \text{BNK\_PRE\%}) * \text{CKE\_LO\_ACT\%}
 \end{aligned}$$

Next the activate power is calculated. This is done with a slight variation to Equation 4, where  $t_{ACT}$  is substituted for  $(t_{ACT} * t_{CK})$ .  $t_{ACT}$  is the average cycle time between ACTIVATE commands to the DRAM.

#### Equation 19

$$p(ACT) = (I_{DD0} - I_{DD3N}) * \frac{t_{RC(spec)}}{t_{ACT}} * V_{DD}$$

Similarly, Equations 6, 9, and 11 are modified to work with RD% and WR% variables.

#### Equation 20

$$p(WR) = (I_{DDW} - I_{DD3N}) * WR\% * V_{DD}$$

$$p(RD) = (I_{DD4R} - I_{DD3N}) * RD\% * V_{DD}$$

$$p(DQ) = p(perDQ) * (num\_of\_DQ + num\_of\_DQS) * RD\%$$

The only other power that is calculated is  $p(REF)$ , as shown in Equation 14. No additional modification is required for  $p(REF)$ .

Now that all the subcomponents of the memory power are calculated, they must be scaled to match the system operating  $V_{DD}$  and operating CK frequency. This is done using Equation 17. Once all the subcomponents are scaled to proper voltage and frequency, they can be added together to provide the total device power consumed.

#### Equation 21

$$P(TOT) = P(PRE\_PDN) + P(PRE\_STBY) + P(ACT\_PDN) \\ + P(ACT\_STBY) + P(WR) + P(RD) + P(DQ) + P(REF)$$

The total power dissipation of a DDR SDRAM operating under specific system usage conditions has now been calculated, with all primary variables that affect device power having been compensated for.

This can be difficult to do without the proper tools. An Excel spreadsheet is available to facilitate DDR SDRAM memory system power calculations at [www.micron.com/systemcalc](http://www.micron.com/systemcalc). To utilize this spreadsheet, enter the device data sheet conditions on the "Device Spec" tab. Then enter the system conditions on the "Usage Conditions" tab (refer to the table on page 8). With this information, all of the powers are calculated, the intermittent results shown on the "Power Calcs" tab and the final results displayed on the "Summary" page. (See Appendix A for examples.)

## SUMMARY

At first glance at the data sheet, it is difficult to determine how much power a DDR SDRAM will consume in a system environment. However, by understanding the data sheet and how a DDR SDRAM consumes power, it is possible to create a power model based on system usage conditions. A system designer can utilize this model to accurately approximate the power requirements of a DDR SDRAM in a system environment. These results can be used to optimize the system power delivery and thermal budget to optimize performance versus cost of the system.

This model allows a system designer to experiment with various memory access schemes to determine the impact on power consumption. To reduce power, a system designer could consider more aggressive use of power-down (CKE is LOW).

A system designer may also use the model to determine increases in power caused by speculatively opening multiple banks or speculatively reading data from an open row. Both techniques can be used to increase system performance at the cost of higher device power. This tool provides a method for estimating the power increase and for making system architecture and design decisions.

By accurately estimating realistic power consumptions, the system designer is able to handle all system trade-offs to optimize the system for its determined use.

## APPENDIX A: DATA SHEET ASSUMPTIONS

(Note: 1);  $0^{\circ}\text{C} \leq T_A < +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ;  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$

PARAMETER/CONDITION	SYMBOL	-75/-75Z	-8	UNITS	NOTES
OPERATING CURRENT: One bank; Active Precharge; $t_{RC} = t_{RC\ MIN}$ ; $t_{CK} = t_{CK\ MIN}$ ; DQ, DM, and DQS inputs changing once every two clock cycles	$I_{DD0}$	105	100	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK\ MIN}$ ; CKE = LOW	$I_{DD2P}$	3	3	mA	
IDLE STANDBY CURRENT: $CS_{-} = \text{HIGH}$ ; All banks idle; $t_{CK} = t_{CK\ MIN}$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN}$ and $V_{REF}$ for DQ, DQS, and DM	$I_{DD2F}$	45	35	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank; Power-down mode; $t_{CK} = t_{CK\ MIN}$ ; CKE = LOW	$I_{DD3P}$	18	18	mA	
ACTIVE STANDBY CURRENT: $CS_{-} = \text{HIGH}$ ; One bank; $t_{CK} = t_{CK\ MIN}$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN}$ and $V_{REF}$ for DQ, DQS, and DM	$I_{DD3N}$	45	35	mA	
OPERATING CURRENT: Burst = 2; READs; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK\ MIN}$ ; $I_{OUT} = 0\text{mA}$	$I_{DD4R}$	110	90	mA	
OPERATING CURRENT: Burst = 2; WRITEs; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK\ MIN}$ ; DQ, DM, and DQS changing twice per clock cycle	$I_{DD4W}$	110	90	mA	
AUTO REFRESH CURRENT; $t_{RC} = 15.625\mu\text{s}$	$I_{DD5}$	5	5	mA	2

- NOTE:**
- $I_{DD}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 2 for -75Z, -8 and CL = 2.5 for -75 with the outputs open.
  - CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until  $t_{REF}$  later.

## APPENDIX B: EXAMPLES

Two examples are provided to show how to utilize the spreadsheet (see the spreadsheet at: [www.micron.com/systemcalc](http://www.micron.com/systemcalc)). The first is for a device in a PC system with a 100 MHz clock under moderate workload. The second is for a PC system with 133 MHz clock under a high-stress workload.

### DDR200 MODERATE USAGE EXAMPLE

The first example of calculating DDR SDRAM power in a system environment is for a PC1600 system using x8 devices operating at a clock rate of 100 MHz. The system usage conditions are shown in the table below.

VCC	2.5	V
CK Frequency	100	MHz
Output Power	6.88	mW
Percentage of time all banks are precharged	40%	
Percentage of timeCKE LOW during precharge	80%	
Percentage of timeCKE LOW during active	20%	
Average time between ACT commands	120	ns
Percentage of output cycles reading data	30%	
Percentage of output cycles writing data	15%	

The system usage assumes that 40 percent of the time, all banks on the DDR SDRAM are in a precharge state and the average time between ACT commands is 120ns. The controller uses an aggressive power management scheme during precharge state to keep the device in PDN mode 80 percent of the time. During the active state, the device is in PDN mode 20 percent of the time. Under conditions like this, the outputs will not be driving/receiving data at 100 percent bus utilization. Instead, it is assumed that the device drives data 30 percent of the time and receives data 15 percent of the time.

Once these assumptions are input into the spreadsheet, it calculates each subcomponent of power and derates it to the system use condition.

Power Derated for System Usage Conditions Input Into This Model	
p(PRE_PDN)	2.6 mW
p(IDLE_STBY)	9.7 mW
p(ACT_PDN)	5.8 mW
P(ACT_STBY)	58.3 mW
p(REF)	5.4 mW
p(ACT)	81.0 mW
p(WR)	26.3 mW
p(RD)	52.7 mW
p(DQ)	18.6 mW

**Totals** **260.4mW**

These results assume data sheet worst-case  $V_{DD}$  and data sheet  $t_{CK}$  specifications. Then the worksheet scales the power to compensate for actual system  $V_{DD}$  and clock rate, as shown below.

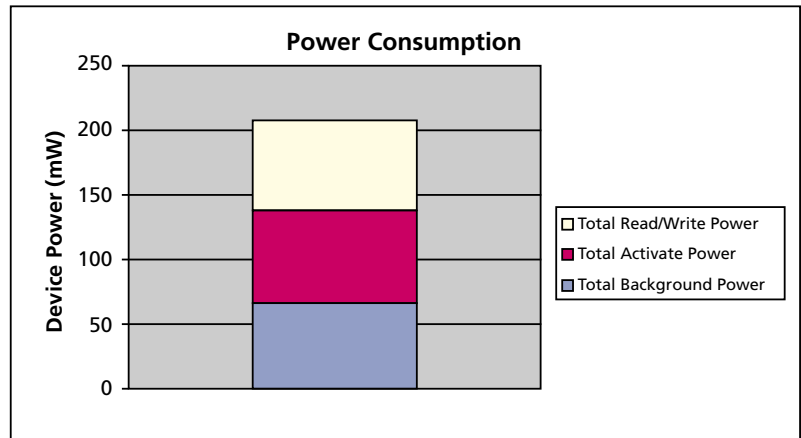
Power Scaled for Actual System CK Frequency and Vcc	
P(PRE_PDN)	2.2 mW
P(IDLE_STBY)	6.3 mW
P(ACT_PDN)	5.0 mW
P(ACT_STBY)	50.0 mW
P(REF)	4.6 mW
P(ACT)	69.4 mW
P(WR)	16.9 mW
P(RD)	33.9 mW
P(DQ)	18.6 mW

**Totals** **206.9mW**

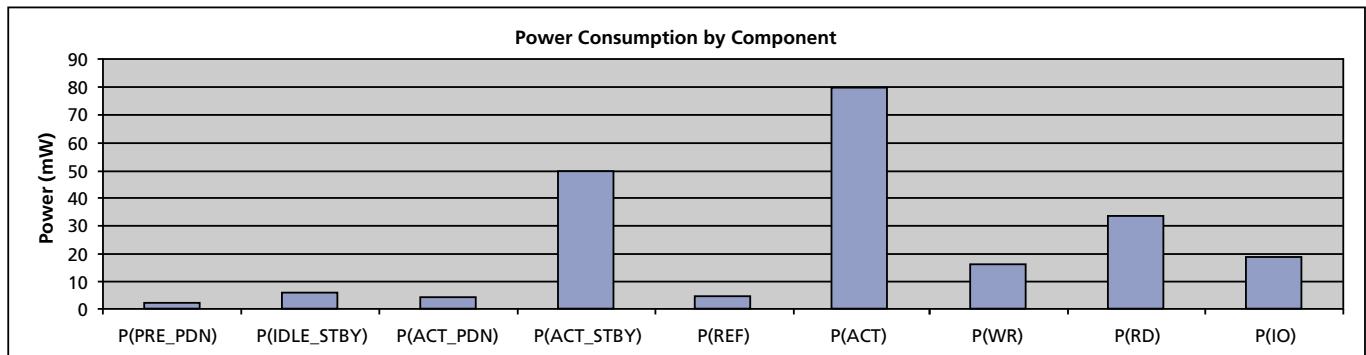
A summary of the results is shown below. Under these system conditions, 68mW of power is used for the background operations, including all power-down, standby, and refresh powers. An average of 69mW is consumed activating banks, while 69mW is consumed actually reading and writing data to the DDR SDRAM. The summation of these powers shows the total device draws ~207mW of power during a typical workload.

**Power Consumption Summary**

P(PRE_PDN)	2.2 mW
P(IDLE_STBY)	6.3 mW
P(ACT_PDN)	5.0 mW
P(ACT_STBY)	50.0 mW
P(REF)	4.6 mW
<b>Total Background Power</b>	<b>68.1 mW</b>
P(ACT)	69.4 mW
<b>Total Activate Power</b>	<b>69.4 mW</b>
P(WR)	16.9 mW
P(RD)	33.9 mW
P(IO)	18.6 mW
<b>Total Read/Write Power</b>	<b>69.4 mW</b>
<b>Total DDR SDRAM Power</b>	<b>206.9 mW</b>



**Power Consumption by Component**



## DDR266 HIGH-STRESS WORKLOAD EXAMPLE

The second example is for a PC2100 system that is operating under a high-stress workload. This type of workload would not normally occur in actual system operation. However, with specific benchmarking software or software designed to stress the memory subsystem, conditions like this may be possible. This condition represents a possible “worst-case” power environment. This type of system is summarized in the following table.

VCC	2.5	V
CK Frequency	133.33	MHz
Output Power	6.88	mW
Percentage of time all banks are precharged	5%	
Percentage of timeCKE LOW during precharge	0%	
Percentage of timeCKE LOW during active	0%	
Average time between ACT commands	30	ns
Percentage of output cycles reading data	80%	
Percentage of ouput cycles writing data	10%	

The clock rate is running at 133 MHz. As the memory is being stressed, the device is reading data out 80 percent of the time, while writing only 10 percent of the time. To support this type of data throughput, the banks are being opened and closed quickly and the average duration between ACT commands is only 30ns. The amount of time when all banks are precharged is assumed to be only 5 percent. The final assumption is that to support these throughputs, there is noCKE power management.

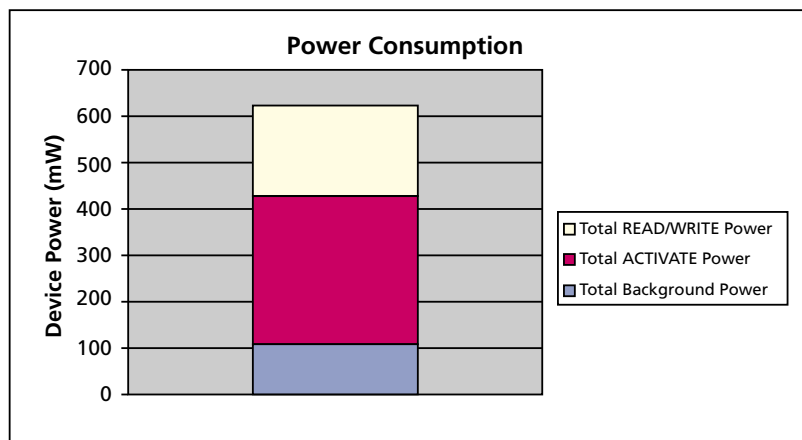
For this analysis, the device data sheet is the same as shown in Appendix A and the previous example.

As shown below, the background power increased to 142mW. This is higher than the previous example because the clock is running at a higher frequency andCKE is not used to enter PDN mode. The activate power increased to 278mW because banks are opened in quick succession with an average ACT-to-ACT time of 30ns, versus 120ns in the previous example. The read/write power also increased to 185mW due to the higher bus utilization of read data.

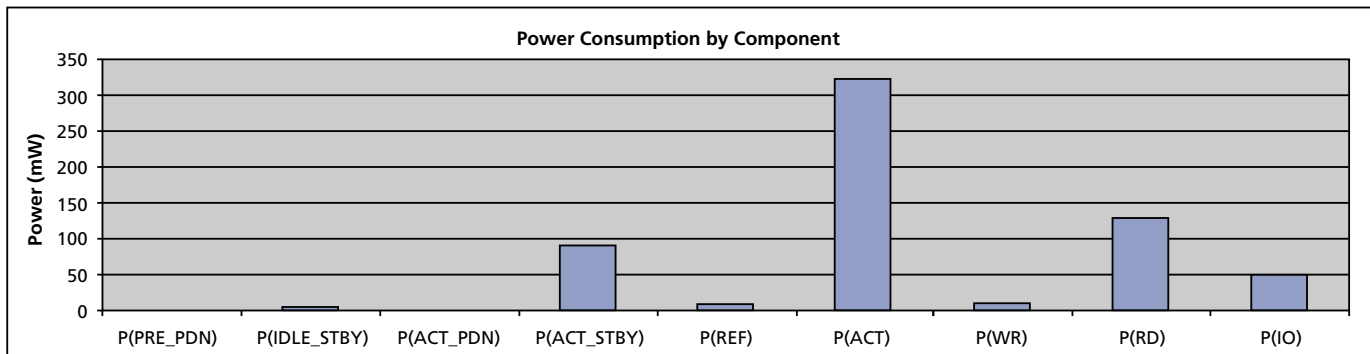
These two examples have shown how a power component can be calculated for a typical usage condition as well as a possible worst-case usage condition.

**Power Consumption Summary**

P(PRE_PDND)	0.0	mW
P(IDLE_STBY)	4.6	mW
P(ACT_PDND)	0.0	mW
P(ACT_STBY)	88.0	mW
P(REF)	11.6	mW
<b>Total Background Power</b>	<b>104.2</b>	<b>mW</b>
P(ACT)	324.1	mW
<b>Total ACTIVATE Power</b>	<b>324.1</b>	<b>mW</b>
P(WR)	12.7	mW
P(RD)	129.6	mW
P(IO)	49.5	mW
<b>Total READ/WRITE Power</b>	<b>191.9</b>	<b>mW</b>
<b>Total DDR SDRAM Power</b>	<b>620.1</b>	<b>mW</b>



**Power Consumption by Component**



## APPENDIX C: ADAPTING TO CALCULATE SDRAM SYSTEM POWER

This technical note has discussed calculating the system power for a DDR SDRAM. However, the techniques can be easily adapted to calculating system power for a standard SDRAM. This requires four changes: substitution of standby powers, calculation of  $I_{DD0}$ , substitution for  $I_{DD4W}$  and  $I_{DD4R}$ , and calculation of nonterminated DQ power.

The first difference between SDRAM and DDR SDRAM specifications is that the SDRAM includes only an  $I_{DD2}$  (PRE\_PDN) and  $I_{DD3}$  (ACT\_STBY). However, a close approximation to the DDR power can be calculated using the following equation:

**Equation 22**

$$\begin{aligned} p(\text{PRE\_PDN}) &= I_{DD2} * V_{DD} \\ p(\text{PRE\_STBY}) &= I_{DD3} * V_{DD} \\ p(\text{ACT\_PDN}) &= I_{DD2} * V_{DD} \\ p(\text{ACT\_STBY}) &= I_{DD3} * V_{DD} \end{aligned}$$

The second difference between SDRAM and DDR SDRAM specifications is that SDRAM does not include an  $I_{DD0}$  parameter. However,  $I_{DD1}$  is specified for a burst of 2 READ. Thus,  $I_{DD0}$  is twoCK cycles of read current (based on  $I_{DD4} - I_{DD3}$ ), subtracted from  $I_{DD1}$ . This can be calculated as follows:

**Equation 23**

$$I_{DD0} = \frac{I_{DD1} - (I_{DD4} - I_{DD3}) * 2 * t_{CK}}{t_{RC}}$$

Once the  $I_{DD0}$  is calculated, it is used in the equations the same as for DDR.

The third difference between SDRAM and DDR SDRAM is that only a single  $I_{DD4}$  is given. It is specified for both read and write operating current as follows:

**Equation 24**

$$\begin{aligned} I_{DD4W} &= I_{DD4} \\ I_{DD4R} &= I_{DD4} \end{aligned}$$

The fourth and final difference between SDRAM and DDR SDRAM is the termination of the outputs. The DDR was terminated to  $V_{TT}$  through a resistor. Thus, the worst-case device power was in the DC case when the output was constantly driving a load. For SDRAM the termination is typically only a capacitive load. Thus, the output power is:

**Equation 25**

$$p(\text{perDQ}) = \text{CLOAD} * V_{DD}^2 * \frac{\text{CK freq}}{2}$$

Therefore, an SDRAM operating at  $V_{DD} = 3.3V$ , with a clock rate of 133 MHz, driving a load of 25pF would draw 18mW per DQ.

Once these four conversions from the SDRAM specification to the DDR SDRAM specification are made, the remaining DDR SDRAM equations can be applied to calculate SDRAM power in a system environment. To facilitate the calculations, an Excel spreadsheet is available from the Micron Web site: [www.micron.com/systemcalc](http://www.micron.com/systemcalc). The spreadsheet is similar to the DDR SDRAM spreadsheet.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

E-mail: [prodmktg@micron.com](mailto:prodmktg@micron.com), Internet: <http://www.micron.com>, Customer Comment Line: 800-932-4992

Micron is a registered trademark and the Micron logo and M logo are trademarks of Micron Technology, Inc.