

# Technical Note

## Backward Compatibility for Faster SDRAM

### Introduction

Though their speed grades have increased significantly over several years of design evolution, SDRAM devices are still built to the original industry standard. Many of the older and slower speed grades are obsolete, but faster speed grades replacing them are fully backward compatible for the industry's standard speed grades, PC133. From the conception of SDRAM, Micron has tailored its data sheets for maximum flexibility and compatibility between speed grades. The faster Micron industry standard speed grades are backward compatible with the original slower speed bins. In fact, the faster speed grade parts use the same designs as the slower speed bins, but the fast speeds are tested to tighter limits. This technical note reviews the timing differences between the faster speeds and slower speeds and shows how the faster Micron parts are compatible with the slower parts.

This technical note only covers speed grades and configurations defined by the PC133 and JEDEC standards: x4, x8, and x16 configurations up to 143 MHz at CAS latency 3 (CL = 3).

### AC Timing Parameters

The AC timings listed in all of Micron's data sheets are asymphonious unless they are listed in clock cycles in the units column of the AC timing tables. The timing parameters listed in the data sheet are also independent of the clock frequency being used. The asymphonious timing parameters need to be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge for the appropriate command, regardless of the speed grade. For example, a  $t_{RCD}$  specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks, rounded to 3. Equation 1 covers any case where  $2 < t_{RCD} (MIN) / t_{CK} = 3$ . (The same procedure is used to convert other specification limits from time units to clock cycles.)

(EQ 1)

$$\begin{aligned} \text{Actual clocks required} &= t_{RCD}(\text{Spec}) / \text{Actual clock cycle time} \\ &= 20\text{ns} / 7.5\text{ns} \\ &= 2.7 \text{ clocks} \\ &= 3 \text{ clocks (rounded up to whole number)} \end{aligned}$$

Table 1 illustrates some of the core timing parameters for the x4, x8, and x16 configurations to show their backward compatibility. The -8E speed grade is shown as a reference only. This speed grade has been replaced by the -75 PC133 speed grade.

**Table 1: Comparison of Key Timing Parameters (x4, x8, x16)**

Parameter	-7E	-75	-8E	Units
$t_{CK @ CL3}$	7	7.5	8	ns
$t_{CK @ CL2}$	7.5	10	10	ns
$t_{RP}$	15	20	20	ns
$t_{RDC}$	15	20	20	ns
$t_{RAS}$	37	44	50	ns
$t_{RC}$	60	66	70	ns
$t_{RFC}$	60	66	70	ns
$t_{OH}$	3	3	3	ns
Note: -8E is for reference only				

## Frequency

Unlike DDR, there is no minimum clock frequency for SDRAM regardless of the speed grade. The minimum clock frequency found in the DDR specification results from the DLL being used to align the data and strobe with the clock. SDRAM devices do not use a DLL; therefore, a minimum  $t_{CK}$  restriction is not needed. SDRAM devices can be run at almost any speed as long as the AC timing parameters are met. The two timing parameters that restrict the minimum clock frequency are refresh and  $t_{RAS MAX}$ . This allows the operating frequency to move from the maximum specified in the data sheet well into the kHz range.

## Low Power and Industrial Temperature

Low power and industrial temperature SDRAM devices have been tested to tighter specification. They allow for designs that do not use the extended temperature range or lower self refresh power to use the parts that have been LP or IT tested to increase their flexibility.

## Conclusion

Micron strives for full backward compatibility in its planning, testing, and development. Micron speed grades are 100 percent backward compatible with at the original industry standard speed grade, PC133.

For the latest data sheets and other technical information, please refer to Micron's Web site at [www.micron.com/datasheets](http://www.micron.com/datasheets).



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## Revision History

- Rev. A ..... 10/05
- Initial release