

Technical Note

Using CellularRAM™ Memory to Replace NEC Mobile Specified RAM (μPD46128512)

Introduction

Micron® CellularRAM™ devices are designed to be backward compatible with 6T SRAM early-generation asynchronous and page PSRAM. Designs requiring high speed and low-power operation constitute one market segment where this backward-compatibility is essential. CellularRAM memory also provides an interface compatible with burst NOR Flash that allows designers to take their designs to the next performance level.

NEC Electronics Mobile Specified RAM, μPD46128512, competes in this market segment. This technical note addresses requirements for a design migration from Mobile Specified RAM to CellularRAM devices.

This technical note describes the following:

- Device overview
- Interface change requirements
- Device driver requirements
- Feature differences: Benefits of using CellularRAM memory

Table 1 shows a comparative overview of device features.

Table 1: μPD46128512 and CellularRAM Differences

Function	μPD46128512	Micron	Notes
Power-up - Power-up time	300μs (MIN)	150μs (MAX)	Both default to async mode
Configuration register - Interface type - Access allowed	Software: async and sync WRITE only	Software: async Hardware (CRE): async and sync WRITE and READ	
Burst mode - Latency type - Latency codes	Fixed only Latency codes: 5–10	Both variable and fixed Latency codes: 3–7	
Mixed mode operation	Not supported	Supported	Clock stopped in sync mode
WAIT pin - Logic level - Transition point	Active LOW only 1 clk before data	Active HIGH or LOW 1 clk before or on clk edge	
Partial array refresh (PAR) - Enabling point - Array size	Only when part disabled Full, 1/8, 1/4, and 1/16	Once PAR setting accepted Full, 1/2, 1/4, 1/8, and none	
Low-power options - Deep power-down - TCR	Supported by 0M bit PAR Not stated in data sheet	Supported Yes (full temperature range)	

Device Overview

NEC μ PD46128512

NEC Electronics introduced the μ PD46128512 device to satisfy market demand for a device that would, like Micron CellularRAM devices, integrate a high-speed core technology with a NOR Flash bus.

The μ PD46128512 is an async/page/burst device. The primary target applications are in the mobile device market, including mobile phones, PDAs, and digital still cameras. The main features are:

- Burst NOR Flash interface
- Independent addressing and data buses
- Support for known good die (KGD) and packaged devices

CellularRAM Devices

Micron CellularRAM devices target applications similar to those targeted by NEC with the additional value proposition of the CellularRAM Workgroup specification. This published common specification allows a designer to consider multiple sourcing.

CellularRAM memory, like the μ PD46128512, is based on DRAM technology. It supports a high-speed memory interface, while meeting the additional requirement for low-power operating modes.

CellularRAM features include:

- Support for 16Mb through 256Mb densities
- Small-package-footprint FBGA devices
- KGD devices
- Burst NOR Flash compatible interface
- Asynchronous, page, and high-speed (up to 133 MHz) burst interface
- Low-power options including PAR, low standby current, and DPD mode
- Hidden refresh control

This technical note will compare async/page/burst 128Mb devices; NEC μ PD46128512 and Micron, CR1.5-compliant CellularRAM device MT45W8MW16B.

Interface Change Requirements

This section covers the following topics:

- Power-up considerations and default operational mode
- Async/page mode differences
- Signal definitions
- Burst mode differences
- WAIT pin functionality
- Chip enable (CE2) operation

Power-Up Considerations and Default Operational Mode

Both CellularRAM and μ PD46128512 devices start their internal initialization phases when the core supply rail reaches a valid power level ($V_{CC} = 1.7-1.95V$). At this point, the internal control circuitry begins to initialize, and both devices will be available for the first access, $CE\# = LOW$, as described below.

Table 2: Initialization Time

Device	Time	Default Mode
Micron CellularRAM	150 μ s (MAX)	Asynchronous
μ PD46128512	300 μ s (MIN)	Asynchronous

During this initialization phase, the μ PD46128512 documentation states that, “Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application.” For the CellularRAM device, the configuration register (CR) is loaded with its default data sheet values. Both devices will power up in asynchronous mode by default.

This means that the Micron device can work with the power-up initialization time delay.

Async/Page Mode Differences

Both devices support asynchronous mode (READ/WRITE) and page mode (READ) operations. The only difference in using the page mode READ interface is that the Micron device requires configuration via the refresh configuration register (RCR[7]) to enable this feature. When configured, the two devices work the same in this operating mode.

Signal Definitions

Signals are the same on both devices, with the exception of CE2 (μ PD46128512) and CRE (CellularRAM). The signals definitions vary as follows:

- Chip enable 2 (CE2) is used to enable partial refresh density (PRD).
- Configuration register enable (CRE) is an optional interface to the CR.

Later sections provide details regarding both the device CR and low-power option settings.

Burst Mode Differences

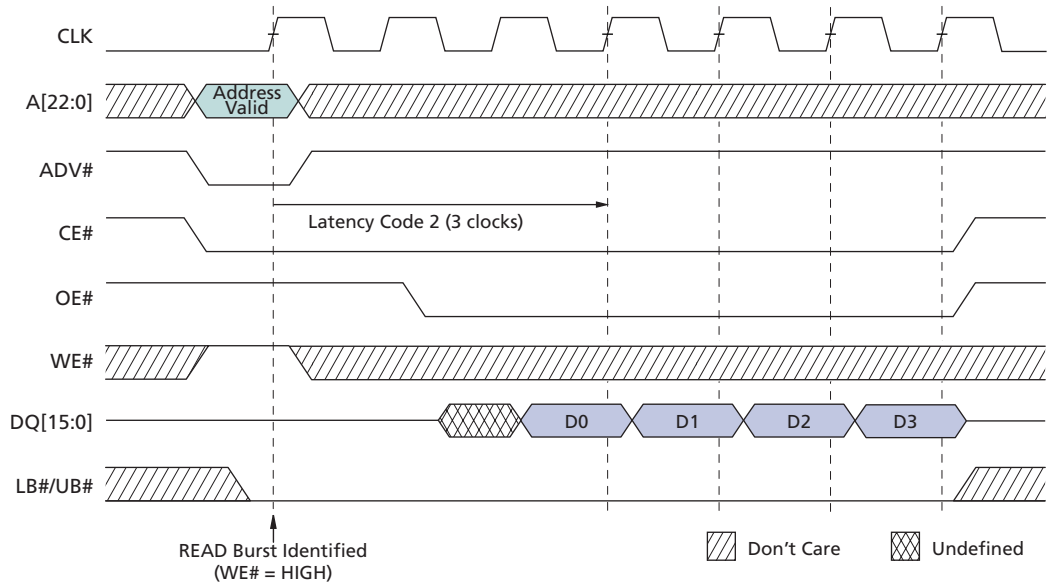
The CellularRAM and μ PD46128512 devices both support the NOR Flash burst control interface (CLK/ADV# and WAIT) and the NOR Flash command sequence. This support can be divided into the following sections:

- Identifying a burst access
- Burst latency codes

Identifying a Burst Access

Figure 1 shows a burst READ and the point at which the burst is identified. This point, the first active edge of CLK where ADV# is LOW, is also the point at which the address is latched and the burst latency starts. This is the same for both the μ PD46128512 and the CellularRAM device. Although not shown, the burst WRITE operation is also identified at this point (WE# LOW).

Figure 1: Burst READ Timing



Burst Latency Codes

Table 3 defines the number of clocks until the data is valid for a given latency code. The main difference between the two devices is that the Micron device uses the same latency code for both the burst READ and burst WRITE operations; for the μ PD46128512, burst WRITE latency = (READ latency - 1). This means that controller support for the burst function can be simplified when using CellularRAM devices.

Table 3: Latency Code Differences

Device	Latency (clocks)	Notes
μ PD46128512	5–10	Fixed latency only
Micron CellularRAM	3–7	Variable and fixed latency

The value programmed into the CR differs between the CellularRAM and μ PD46128512 devices. For the μ PD46128512 device, the MR value—read latency (RL)—is defined as “the number of clock cycles (latency) between the address being latched and the output of the first data in the burst read.” For the CellularRAM device, the CR value—latency count (LC)—is defined as “the number of clock cycles between the beginning of a READ or WRITE operation and the first data value transferred.” Therefore, the CellularRAM CR value should be programmed as $LC = (RL - 1)$.

A controller that monitors WAIT can support either device without a noticeable impact in performance.

WAIT Pin Functionality

As with any burst interface, a signal is necessary to control the “throttling” of the interface between the master (memory controller) and the slave (memory) devices. WAIT provides this function on both devices. The only support differences are detailed in the following section.

Note that all other WAIT polarity and associated timings relative to activating/deactivating WAIT during a burst cycle are the same for both devices.

WAIT Async/Page Operation

The μ PD46128512 device documentation states that “ $\overline{\text{WAIT}}$ output always [stays] high impedance state under asynchronous mode setting.”

The Micron device will drive WAIT during this operational mode but should be ignored as stated.

WAIT Burst Operation

The μ PD46128512 device drives $\overline{\text{WAIT}}$ differently depending on whether it is in a burst READ or WRITE operation.

For the μ PD46128512 burst READ $\overline{\text{WAIT}}$, output is driven LOW when the cycle starts and then will be driven HIGH one clock cycle before the data is ready. Once the burst completes, $\overline{\text{WAIT}}$ is driven High-Z.

For the μ PD46128512 burst WRITE $\overline{\text{WAIT}}$, output is driven HIGH when the cycle starts and remains at that level for the duration of the cycle. Once the burst completes, $\overline{\text{WAIT}}$ is driven High-Z.

The CellularRAM device drives WAIT polarity depending on the value in BCR[10] and is consistent across both burst READ and WRITE operations.

This means that the Micron device can work with the μ PD46128512 $\overline{\text{WAIT}}$ functionality if $\overline{\text{WAIT}}$ is set for active LOW (BCR[10] = 0). Because this is not the default setting, it will need to be configured via the CR.

WAIT vs. Data Ready Driving (BCR[8])

The μ PD46128512 device will always drive $\overline{\text{WAIT}}$ to a deasserted state one clock cycle prior to when data is ready on a burst READ operation. The Micron device can be configured to match the μ PD46128512 device or to drive WAIT to a deasserted state on the clock cycle where data is ready. This is configured via BCR[8].

The two devices can be configured to the same active level by using BCR[8] = 1.

Chip Enable (CE2) Operation

The μ PD46128512 CE2 input controls the enabling of the low-power partial refresh density settings. During normal operations this input must be active HIGH for the μ PD46128512 to function correctly.

The equivalent input on the CellularRAM device, CRE, is only active (HIGH) during access to the configuration registers in hardware mode. For normal operations, this input must be held LOW, so a change to the device driver supporting the CE2 input will be required to support the CellularRAM device CRE input.

Enabling Partial Refresh Density (PRD)

To enable the μ PD46128512 PRD settings, the device must be disabled (/CE1 HIGH) while CE2 is deasserted (LOW). This low-power PRD state will only continue while the part is disabled. Any refresh occurring while CE2 = HIGH will result in a full array refresh.

The CellularRAM device does not require this two-stage operation. Once the PAR settings are enabled in the appropriate CR via the RCR, these PAR settings will be used any time the device refreshes. See “Partial Array Refresh (PAR)” on page 7 for further discussion.

The CellularRAM PAR implementation functions with the noted implementation of the CE2 signal. For example the PAR setting will already be enabled on the CellularRAM device. This combination of CRE/CE# does not affect CellularRAM device functionality.

Device Driver Changes

Previous sections discussed the differences between the μ PD46128512 and CellularRAM devices in terms of hardware connectivity. The software differences between the two devices include the following areas:

- Burst options
- Access to the configuration registers
- CE2 functionality
- Low-power configuration settings

Burst Options

As previously noted, some burst operation differences exist between the μ PD46128512 and CellularRAM devices. The primary software differences are:

- Latency code programming to match the access time required by the memory controller for clock speed and the number of clock cycles to valid data
- WAIT driving/polarity and valid drive strength options differences

Noted differences can be minimized by a memory controller supporting the appropriate WAIT pin functionality.

Access to the Configuration Register

The μ PD46128512 device supports a six-cycle software sequence to setup both portions of the mode register as detailed below.

Table 4: μ PD46128512 Configuration Sequence

Cycle #	Operation	Address	Data
1	READ	7FFFFFFh (MSB)	Read data (RDa)
2	WRITE	7FFFFFFh	RDa
3	WRITE	7FFFFFFh	RDa
4	WRITE	7FFFFFFh	Code 1
5	WRITE	7FFFFFFh	Code 2
6	READ	“Don’t Care”	Read data (RDb)

This operational sequence is very close to the CellularRAM device’s four-cycle software sequence shown in Table 5

Table 5: Software-Controlled Configuration Sequence

Cycle #	Operation	Address	Data
1	READ	MAX address	X
2	READ	MAX address	X
3	WRITE	MAX address	Register select
4	WRITE READ	MAX address MAX address	Configuration value in Configuration value out

The CellularRAM device also offers other options to control the CR. These options are detailed in “CellularRAM Device Interface Improvements and Advantages” on page 8.

Overall, the software algorithm requires minimal changes to support software-enabled access to the CellularRAM device CRs.

CE2 Functionality

Although previously discussed, the modifications needed to support CRE instead of CE2 may require a device driver change since the input may be driven from a configurable output from the memory controller. If this is the case, the polarity change may require a change to the output definition.

Low-Power Configuration Settings

Partial Array Refresh (PAR)

Both devices support an array size reduction that is actively refreshed, thus reducing refresh current consumption. This is called partial refresh density (PRD) in the μ PD46128512 and partial array refresh (PAR) in the CellularRAM device.

Although both devices support a reduction in the array under active refresh, the setting changes in the CellularRAM device will take effect after the WRITE access to the RCR occurs. In the μ PD46128512 device, these setting changes will only take effect when the CE2 input is LOW with CE1 HIGH.

Deep Power-Down (DPD)

Both devices support a feature whereby the lowest possible current consumption mode can be enabled. This mode—“0M bit array refresh density” (μ PD46128512) or deep power-down (CellularRAM)—results in no refresh occurring on the array and allows the current consumption of the device to be in the 10 μ A range. To exit from this mode into normal operation, the system must support a delay to allow the device to initialize; see Table 2.

Feature Differences: Benefits of Using CellularRAM Memory

Unsupported μ PD46128512 Features

The only features of the μ PD46128512 that cannot be supported on the CellularRAM device are:

- Burst READ suspend support via the control of OE# during the cycle (the CellularRAM device can support burst READ suspend operations by stopping the active CLK)
- Burst WRITE suspend support via the control of WE# during the cycle
- Software access to the configuration register (it is limited to asynchronous operating mode only)
- Burst READ/single WRITE support via the CR (the CellularRAM device supports either a full burst or asynchronous access)

CellularRAM Device Interface Improvements and Advantages

CellularRAM devices support a variety of useful options for customer applications, including the capabilities listed below:

- Configuration register access
- Latency modes
- Burst operation
- Low-power options

Configuration Register Access

READ and WRITE Access to the Configuration Registers

The CellularRAM device supports both READ and WRITE access to the three configuration registers on the device:

- Burst configuration register (BCR)
- Refresh configuration register (RCR)
- Device ID register (DIDR)

The DIDR enables designers to obtain information pertaining to the device they are accessing via software methods. Information such as manufacturer, device revision, and device density are available from this read-only register.

Hardware Access to the Configuration Registers

The three CellularRAM configuration registers can be accessed in a hardware- or software-initiated mode. The hardware method, not available on the μ PD46128512 device, enables READ and WRITE access to the CR. The CellularRAM data sheet contains the full definition of this interface.

This function can be performed in both asynchronous and synchronous operating modes.

Configuration Register Default values

The μ PD46128512 mode register has no power-up default values except that the device is configured for asynchronous operation. Therefore, the device driver must access and set the MR after the initialization period. The μ PD46128512 data sheet does not describe the correct MR settings for asynchronous operation.

When reconfiguring the CellularRAM device for asynchronous operation (BCR[15] = 1), the device driver must only change the required BCR settings. All other BCR values can remain unchanged, as they will be ignored.

Latency Modes

The CellularRAM device supports both variable and fixed latency modes. Both latency modes offer benefits that depend on memory controller requirements and the CellularRAM device interface.

Variable Latency

Variable latency is the ability of a device to work at the highest performance levels via WAIT and still maintain the ability to refresh as required. A pending refresh is signaled to the memory controller with WAIT. If a refresh is required, the push-out delay in the deassertion of WAIT only occurs after the refresh is complete. This push-out only occurs at the start of a cycle that has a refresh pending; on other cycles, WAIT will not experience a push-out of WAIT deassertion.

Fixed Latency

Fixed latency is provided to guarantee timing to the first access by enabling a refresh opportunity at the start of every burst cycle. By providing a refresh opportunity, the first access is delayed by a defined period on both burst READs and WRITEs, thus eliminating the need to monitor WAIT.

Burst Operation

Modes Supported

By using mixed-mode operation, the CellularRAM device supports any combination of burst and asynchronous READ or WRITE operations in synchronous mode ($BCR[15] = 0$).

The Micron device adds support for a burst length of 32 words via $BCR[2:0]$. This is in addition to the standard 4-, 8-, and 16-word burst lengths and continuous burst modes.

An option is also provided to wrap or not wrap within a defined burst length using $BCR[3]$.

Mixed Mode Operation

The ability of a device to switch between synchronous and asynchronous operational modes is called “mixed mode.”

Mixed mode operation with a $\mu PD46128512$ -based design requires the software driver to switch modes, reconfiguring the MR from synchronous to asynchronous operation via M (DQ5).

Mixed mode operation with a Micron CellularRAM design is much easier, since the CellularRAM device allows the design to remain configured for synchronous mode operation, $BCR[15] = 0$. In this mode, the CellularRAM device can operate in the asynchronous mode just by stopping the CLK input. This simplifies the device driver and allows the device to stay configured for synchronous mode.

Low-Power Options

Temperature-Compensated Refresh (TCR)

The CellularRAM device supports multiple internal TCR settings across the supported device temperature range. This ensures that the refresh rate is adjusted according to the operating temperature.

Partial Array Refresh

The CellularRAM device gives customers more options when using PAR to reduce the refresh current by increasing the number of areas of the device that can be refreshed.

Deep Power-Down

The CellularRAM device gives customers better control when enabling DPD. This mode, as mentioned previously, is the same as the μ PD46128512 “PRD = 0M bit” but splitting the CellularRAM PAR and DPD registers from the other burst options provides greater flexibility for the designer.

Memory Block Diagrams

When replacing a μ PD46128512 device with a CellularRAM device, it is necessary to understand the connections required between the memory controller and the CellularRAM device (see Figures 2 and 3).

Figure 2: μ PD46128512 Device Connection to Memory Controller

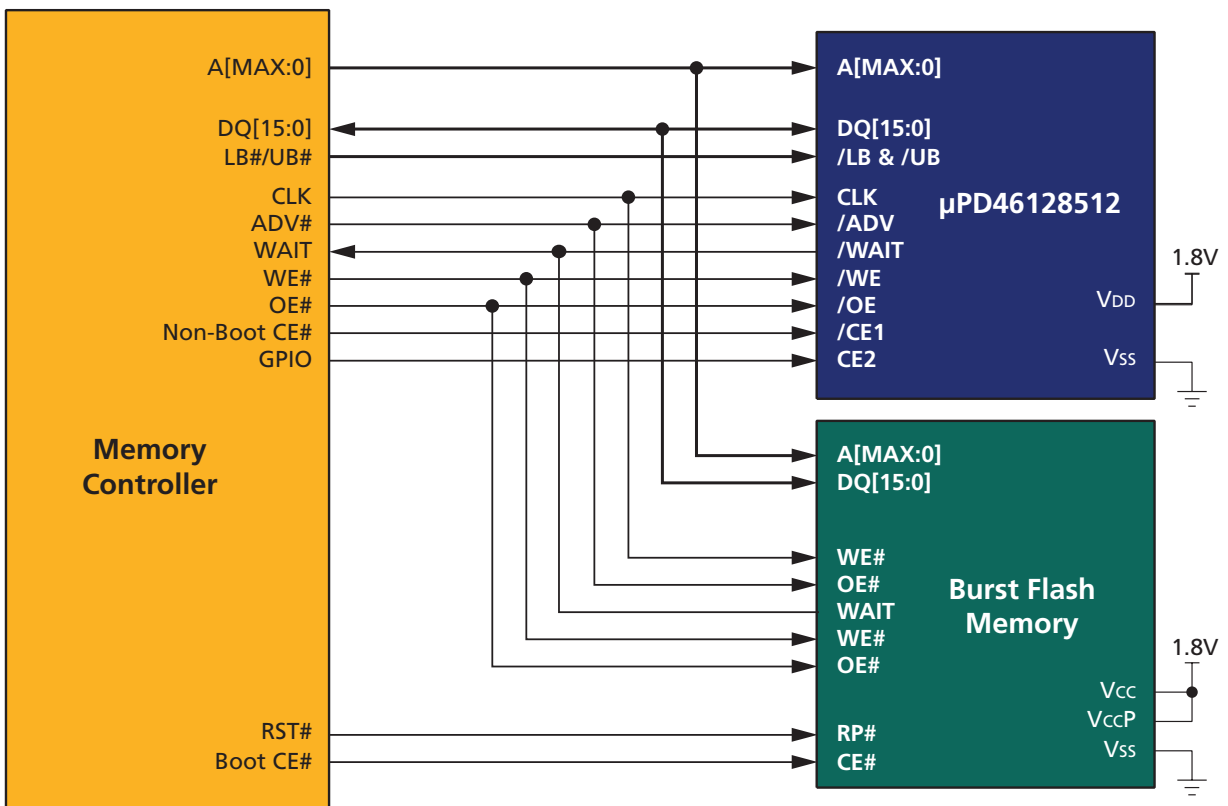
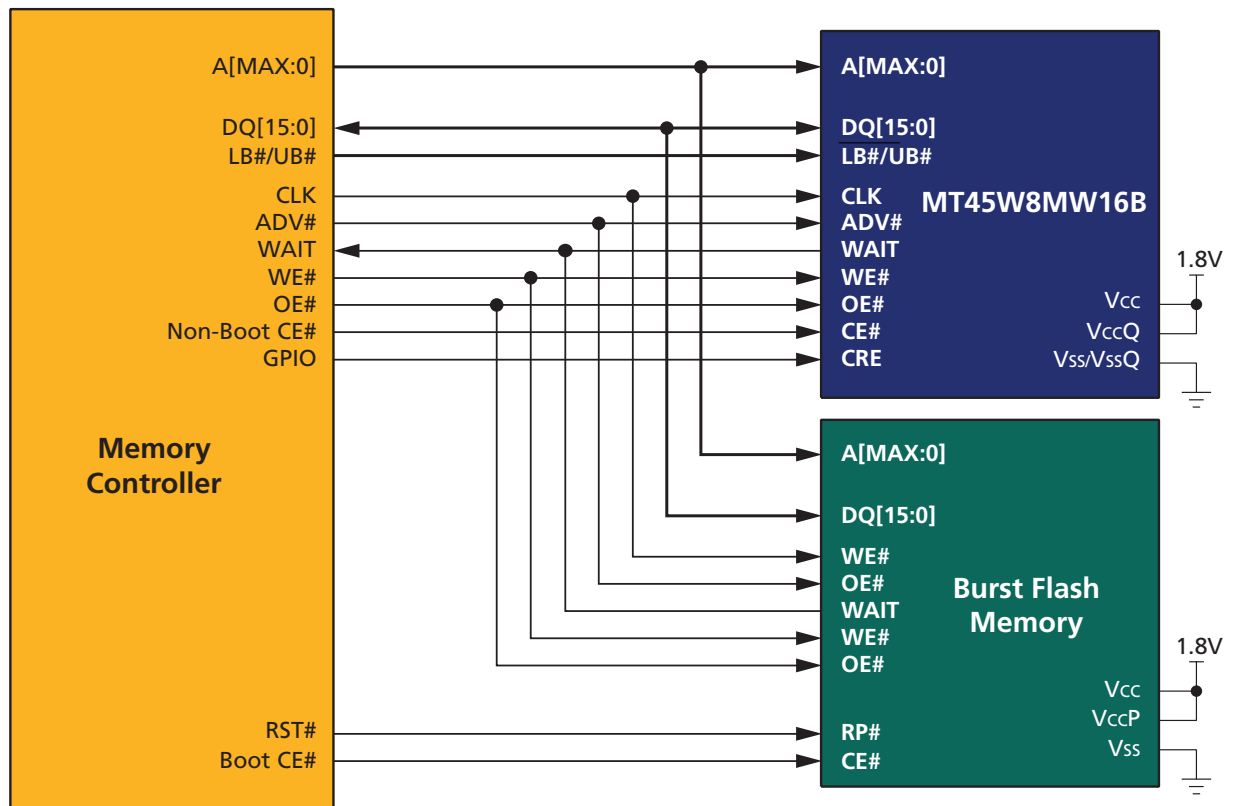


Figure 3: CellularRAM Device Connection to Memory Controller



Conclusion

This technical note shows areas of the current design that must be examined when considering a transition to Micron CellularRAM devices. These changes can be grouped together into the following areas:

- Configuring the CellularRAM device
- Burst latency configuration
- Memory controller/CellularRAM device interface connections

For technical assistance, e-mail psramsupport@micron.com or visit Micron’s Web site: www.micron.com/products/psram/.

References

- NEC μ PD46128512 data sheet—MB82DBR08163A (<http://www.necel.com/memory/en/download/M17507EJ2V0DS00.pdf>)
- Micron CellularRAM—MT45W8MW16B (<http://download.micron.com/pdf/datasheets/psram/>)



Revision History

Rev. 1.0 3/06

- Initial release



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