

Technical Note

DDR2 Simulation Support

Introduction

Micron provides extensive design support tools for system designers. For example, Micron’s recently released technical note “DDR2-533 Memory Design Guide for Two-DIMM Unbuffered Systems,” (TN-47-01) enables board designers to develop a set of general design rules and then, through simulation, verify the design in their particular environments. It is available on Micron’s Web site at <http://www.micron.com/products/dram/ddr2sdram/technote.html>.

Designers can also use Micron’s proprietary DDR2 2-slot-per-channel simulation tool to quickly evaluate alternatives for the common design schematic of DDR2 devices that have two slots per memory channel.

Figures 1, 2, and 3 depict the simulator’s operation and output. Figure 1 illustrates the tool’s control bar, through which engineers define variables that can be altered and by what values. Figure 2 is a schematic of the memory channel being simulated, and Figure 3 shows examples of the simulator’s output, which provides data on jitter, minimum slew rate, and the data eye aperture for each slot and condition—dual-rank (2R), single-rank (1R), and empty (e).

Figure 1: DDR2 2-Slot-per-Channel Simulation Control Bar

| Operation | Data Rate | RON Controller | RON DRAM | MB Zo | MB Lead-in | DRAM ODT | Controller ODT | Cdev | |
|--|---|--|---|--|--|---|---|--|---|
| <input checked="" type="radio"/> READ <input type="radio"/> WRITE | <input checked="" type="radio"/> 533 MB/s <input type="radio"/> 667 MB/s <input type="radio"/> 800 MB/s | <input type="radio"/> 20 ohms <input checked="" type="radio"/> 35 ohms <input type="radio"/> 50 ohms | <input type="radio"/> 8 ohms <input checked="" type="radio"/> 18 ohms <input type="radio"/> 28 ohms | <input type="radio"/> 39 ohms <input checked="" type="radio"/> 50 ohms <input type="radio"/> 60 ohms | <input type="radio"/> 2500 mils <input checked="" type="radio"/> 3500 mils <input type="radio"/> 4500 mils | <input type="radio"/> 100/50 ohms <input checked="" type="radio"/> 150/75 ohms <input type="radio"/> 200/100 ohms | <input type="radio"/> 100/50 ohms <input checked="" type="radio"/> 150/75 ohms <input type="radio"/> 200/100 ohms | <input type="radio"/> 3.0pF <input checked="" type="radio"/> 3.5pF <input type="radio"/> 4.0pF | <input type="button" value="View Simulation"/> <input type="button" value="View Schematic"/> <input type="button" value="ODT Table"/> |

Figure 2: DDR2 2-Slot-per-Channel Simulation Schematic

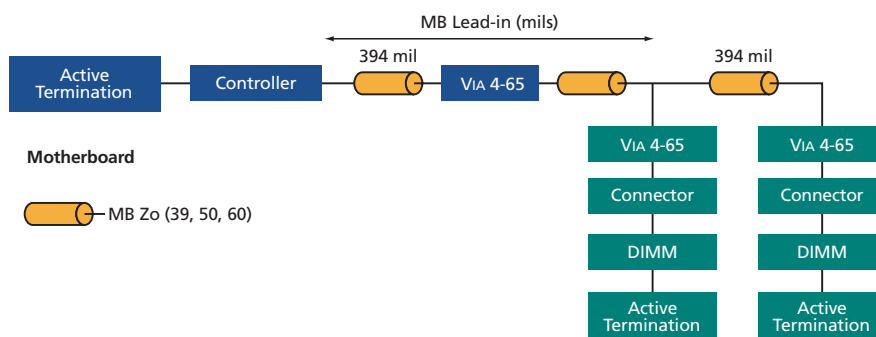
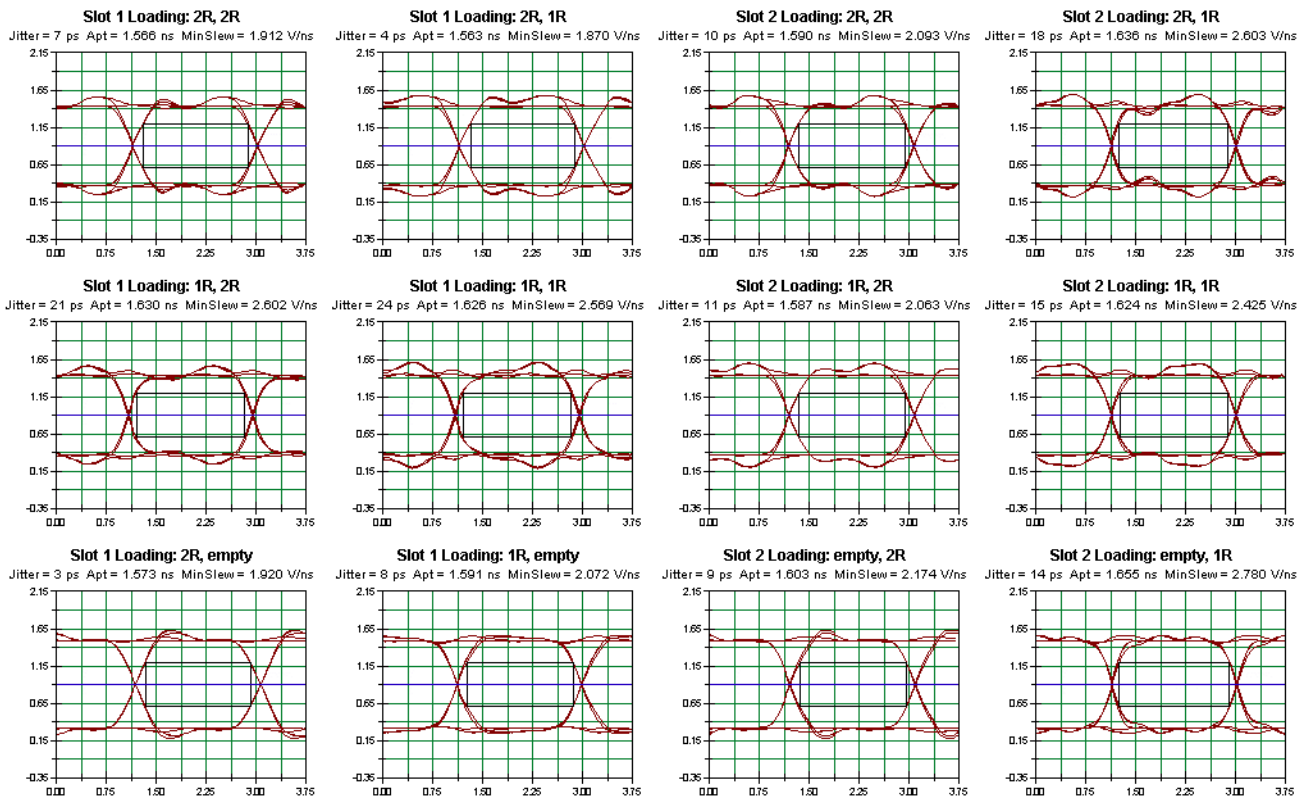


Figure 3: DDR2 2-Slot-per-Channel Simulation Printout



After performing several simulations comparing motherboard impedances (39 ohms versus 50 ohms) and on-die termination (ODT) settings (150 ohms/75 ohms versus 100 ohms/50 ohms), the apertures of the data eye were recorded (Table 1). The results show an improvement of slightly less than 50 picoseconds (ps) when using the optional 100-ohm/50-ohm ODT instead of the standard 150-ohm/75-ohm ODT.

The ODT setting of 150 ohms/75 ohms is dependent on the memory channel's type of access and loading configuration. Table 2 shows Micron's recommended setup for ODT control during READ operations, and Table 3 shows Micron's recommended setup for ODT control during WRITE operations.

This DDR2 simulation tool is not available on the Micron Web site. Access can be made available to customers on an as-requested basis.

Table 1: DDR2 2-Slot-per-Channel Simulations

| Operation | Data Rate (MT/S) | RON (ohms) | | MB Zo (ohms) | MB Lead-in (ohms) | ODT (ohms) | |
|-----------|------------------|------------|------|--------------|-------------------|------------|--------|
| | | Controller | DRAM | | | Controller | DRAM |
| READ | 533 | 35 | 18 | 39 | 3,500 | 150/75 | 150/75 |
| READ | 533 | 35 | 18 | 50 | 3,500 | 150/75 | 150/75 |
| READ | 533 | 35 | 18 | 39 | 3,500 | 100/50 | 100/50 |
| READ | 533 | 35 | 18 | 50 | 3,500 | 100/50 | 100/50 |
| WRITE | 533 | 35 | 18 | 39 | 3,500 | 150/75 | 150/75 |
| WRITE | 533 | 35 | 18 | 50 | 3,500 | 150/75 | 150/75 |
| WRITE | 533 | 35 | 18 | 39 | 3,500 | 100/50 | 100/50 |
| WRITE | 533 | 35 | 18 | 50 | 3,500 | 100/50 | 100/50 |

| Operation | CDEV (pf) | Smallest Data Eye | | Largest Data Eye | |
|-----------|-----------|-------------------|-----------------------|------------------|-----------------------|
| | | Aperture (ns) | Configuration Loading | Aperture (ns) | Configuration Loading |
| READ | 4 | 1.569 | Slot 2 (2R,1R) | 1.654 | Slot 2 (e,1R) |
| READ | 4 | 1.563 | Slot 2 (2R,1R) | 1.655 | Slot 2 (e,1R) |
| READ | 4 | 1.525 | Slot 2 (2R,1R) | 1.624 | Slot 2 (e,1R) |
| READ | 4 | 1.516 | Slot 2 (2R,1R) | 1.618 | Slot 2 (e,1R) |
| WRITE | 4 | 1.377 | Slot 2 (2R, 2R) | 1.649 | Slot 2 (2R,1R) |
| WRITE | 4 | 1.268 | Slot 2 (2R, 2R) | 1.618 | Slot 2 (e,1R) |
| WRITE | 4 | 1.422 | Slot 2 (2R, 2R) | 1.655 | Slot 2 (2R,1R) |
| WRITE | 4 | 1.317 | Slot 2 (2R, 2R) | 1.633 | Slot 2 (2R,1R) |

Table 2: ODT Control During READs

| Configuration | | Read From | DQ Active to ODT RESISTANCE | | | | |
|---------------|--------|-----------|-----------------------------|----------------|-----------|----------------|-----------|
| Slot 1 | Slot 2 | | Controller | DRAM at Slot 1 | | DRAM at Slot 2 | |
| | | | | Front Side | Back Side | Front Side | Back Side |
| DR | DR | Slot 1 | 150Ω | ODT off | ODT off | 75Ω | ODT off |
| | | Slot 2 | 150Ω | 75Ω | ODT off | ODT off | ODT off |
| DR | SR | Slot 1 | 150Ω | ODT off | ODT off | 75Ω | n/a |
| | | Slot 2 | 150Ω | 75Ω | ODT off | ODT off | n/a |
| SR | DR | Slot 1 | 150Ω | ODT off | n/a | 75Ω | ODT off |
| | | Slot 2 | 150Ω | 75Ω | n/a | ODT off | ODT off |
| SR | SR | Slot 1 | 150Ω | ODT off | n/a | 75Ω | n/a |
| | | Slot 2 | 150Ω | 75Ω | n/a | ODT off | n/a |
| DR | Empty | Slot 1 | 75Ω | ODT off | ODT off | n/a | n/a |
| Empty | DR | Slot 2 | 75Ω | n/a | n/a | ODT off | ODT off |
| SR | Empty | Slot 1 | 75Ω | ODT off | n/a | n/a | n/a |
| Empty | SR | Slot 2 | 75Ω | n/a | n/a | ODT off | n/a |

Note: DR = Dual-Rank
SR = Single-Rank

Table 3: ODT Control During WRITES

| Configuration | | Write To | Controller | DQ Active to oDT RESISTANCE | | | |
|---------------|--------|----------|------------|-----------------------------|-----------|----------------|-----------|
| Slot 1 | Slot 2 | | | DRAM at Slot 1 | | DRAM at Slot 2 | |
| | | | | Front Side | Back Side | Front Side | Back Side |
| DR | DR | Slot 1 | ODT off | ODT off | ODT off | 75Ω | ODT off |
| | | Slot 2 | ODT off | 75Ω | ODT off | ODT off | ODT off |
| DR | SR | Slot 1 | ODT off | ODT off | ODT off | 75Ω | n/a |
| | | Slot 2 | ODT off | 75Ω | ODT off | ODT off | n/a |
| SR | DR | Slot 1 | ODT off | ODT off | n/a | 75Ω | ODT off |
| | | Slot 2 | ODT off | 75Ω | n/a | ODT off | ODT off |
| SR | SR | Slot 1 | ODT off | ODT off | n/a | 75Ω | n/a |
| | | Slot 2 | ODT off | 75Ω | n/a | ODT off | n/a |
| DR | Empty | Slot 1 | ODT off | 150Ω | ODT off | n/a | n/a |
| Empty | DR | Slot 2 | ODT off | n/a | n/a | 150Ω | ODT off |
| SR | Empty | Slot 1 | ODT off | 150Ω | n/a | n/a | n/a |
| Empty | SR | Slot 2 | ODT off | n/a | n/a | 150Ω | n/a |

Note: DR = Dual-Rank
SR = Single-Rank

Summary

Micron not only supports its customers with the most current DDR2 component and module specifications, it provides unparalleled DDR2 design tools, such as the DDR2 Memory Design Guide and the DDR2 DQ Eye Simulator.



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