

Technical Note

Advantages of DDR2 Differential DQS Signaling

Introduction

This technical note focuses specifically on the benefits the new differential DQS signaling feature provides and explains how to design with it. Compared with single-ended DQS signaling, which makes it more difficult to obtain accurate data strobing, differential DQS signaling improves data rate operation, particularly for DDR2-667, DDR2-800, and DDR2-1066. With improvements in data capture timing across voltage and temperature fluctuations in the system, the advantages of differential DQS signaling make it a good choice for system designs.

Note: Differential DQS signaling is an optional feature that must be enabled in DDR2 devices. To enable DQS#, bit E10 must be set to “0” in the extended mode register (EMR1). For more information, visit micron.com.

Advantages of Differential DQS Signaling

Primary advantages of differential DQS signaling in DDR2-667, DDR2-800, and DDR2-1066 systems include:

- Reduced crosstalk, which is common-mode interference between true and complementary clock signals
- Reduced simultaneous switching output (SSO) noise in the DQS/DQS# output driver
- Reduced electromagnetic interference (EMI) because DQS and DQS# signaling cancel each other's EMI effect

Other advantages of differential DQS signaling include:

- DQS output pulse width is less dependent on the operating voltage and temperature. The difference between rising and falling slew rates causes less DQS duty cycle distortion.
- DQSQ (DQS-DQ skew) is more tightly controlled. Less derating is required than with single-ended DQS.
- t_{DS}^t/t_{DH}^t specifications are easier to satisfy. Less uncertainty exists when DQS switches because there is only one reference point (DQS/DQS# cross point), whereas single-ended DQS uses two reference points (DQS rising and falling across V_{REF}).

Although this technical note will focus on the advantages that differential DQS signaling offers, it should be noted that differential DQS signaling does have some minor drawbacks, including the need for additional pins and layout space and increased power.

DQS Output Pulse Width Improvements

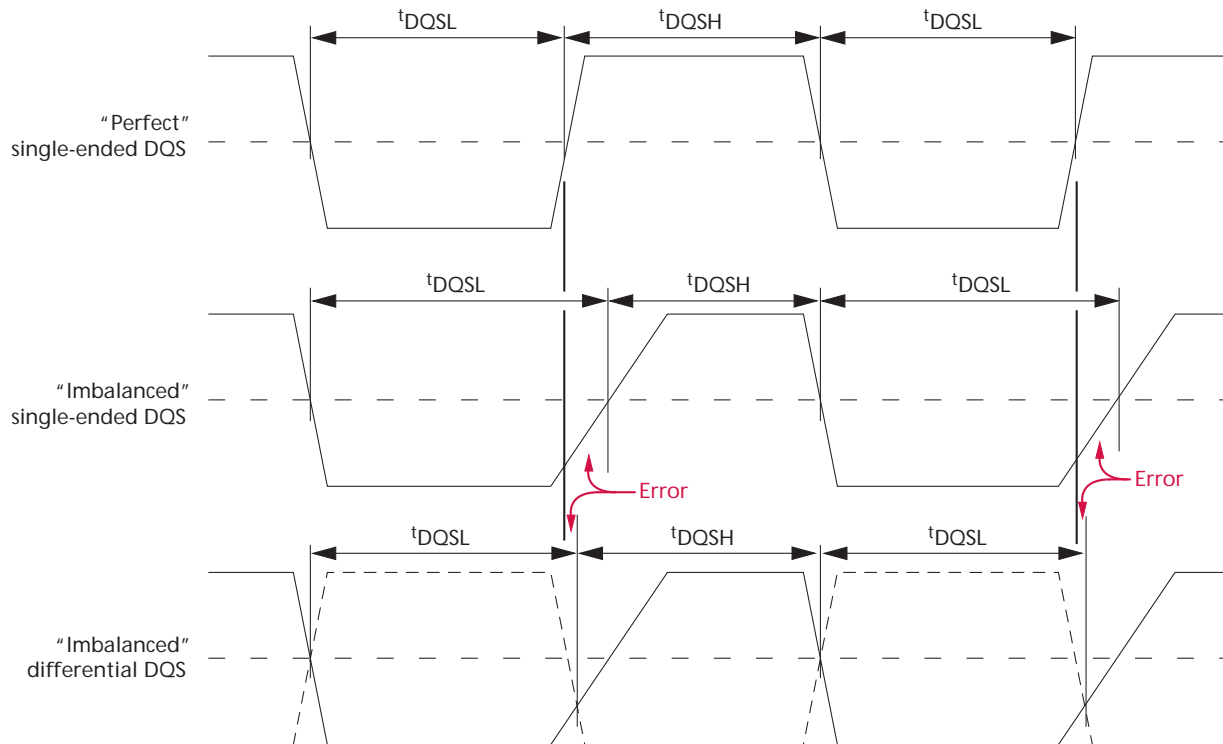
DQS pulse width provides two improvements: reduced DQS duty fluctuations and wider memory controller DQS input.

DQS Duty Fluctuation

Pulse width is defined as DQS/DQS# crossing point to DQS/DQS# crossing point. The cross point position can vary, but the pulse width will not. Because pulse width is not significantly affected by rising and falling slew rates, differential DQS signaling can reduce distortion of the DQS output duty ratio caused by imbalance between the pull-up and the pull-down drivers. Slew rate variations are caused by process parameters, operation voltage, SSO, and temperature changes.

With single-ended DQS, slow rising and fast falling skew rates make t_{DQSL} wider and t_{DQSH} narrower, which can induce duty cycle distortion. With differential DQS/DQS# signaling, the difference between rising and falling DQS slew rates does not cause significant DQS duty cycle distortion (see Figure 1).

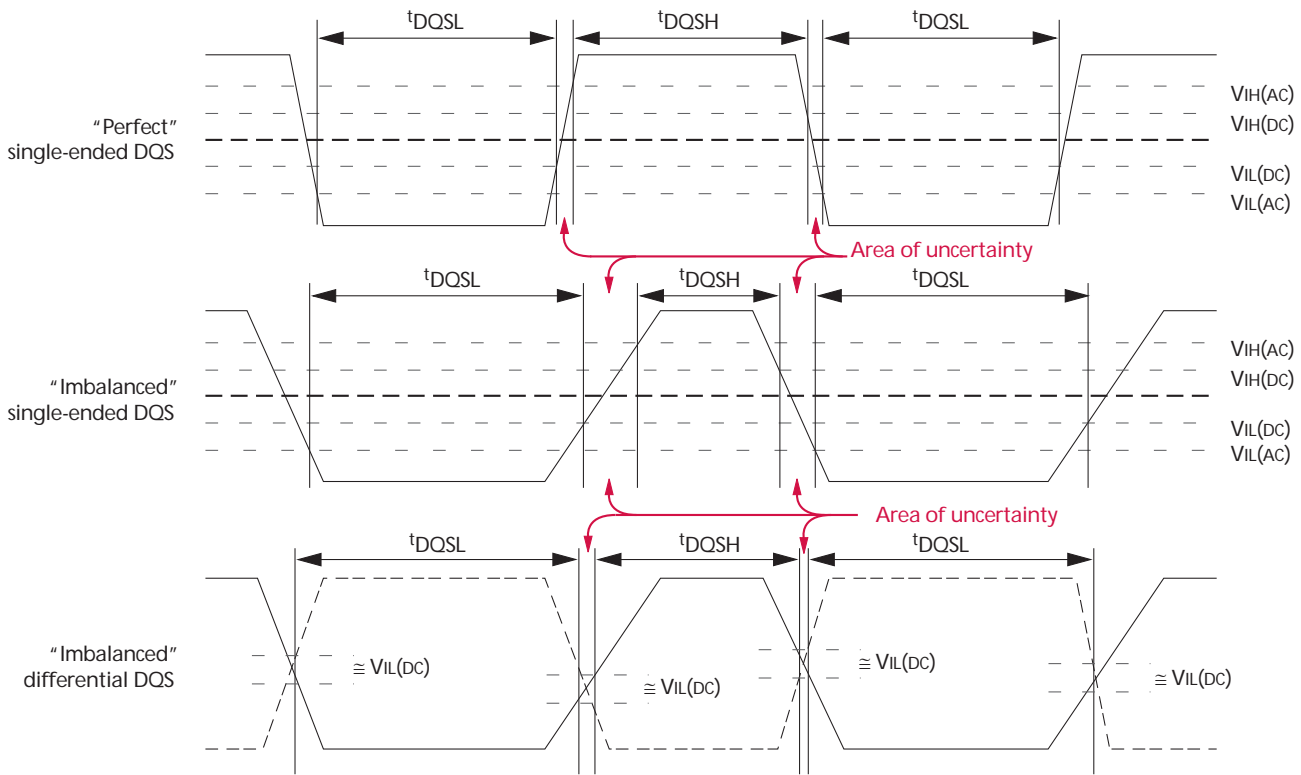
Figure 1: Duty Cycle Variation



Wider Memory Controller DQS Input

The memory controller input specifications have an area of uncertainty where the input is not defined as “H” nor “L.” This area of uncertainty can be reduced with differential DQS output; this is especially true with slew rates. For single-ended DQS, slower slew rates increase the area of uncertainty. For differential DQS, the faster slew rates of DQS and DQS# result in less area of uncertainty. Thus, the DQS pulse width (based on the receiver input specification) becomes relatively larger than with single-ended DQS. As shown in Figure 2 on page 3, the area of uncertainty is between $V_{IL}(DC)$ and $V_{IH}(AC)$ for a rising edge and $V_{IH}(DC)$ and $V_{IL}(AC)$ for a falling edge.

Figure 2: DQS Pulse to Memory Controller



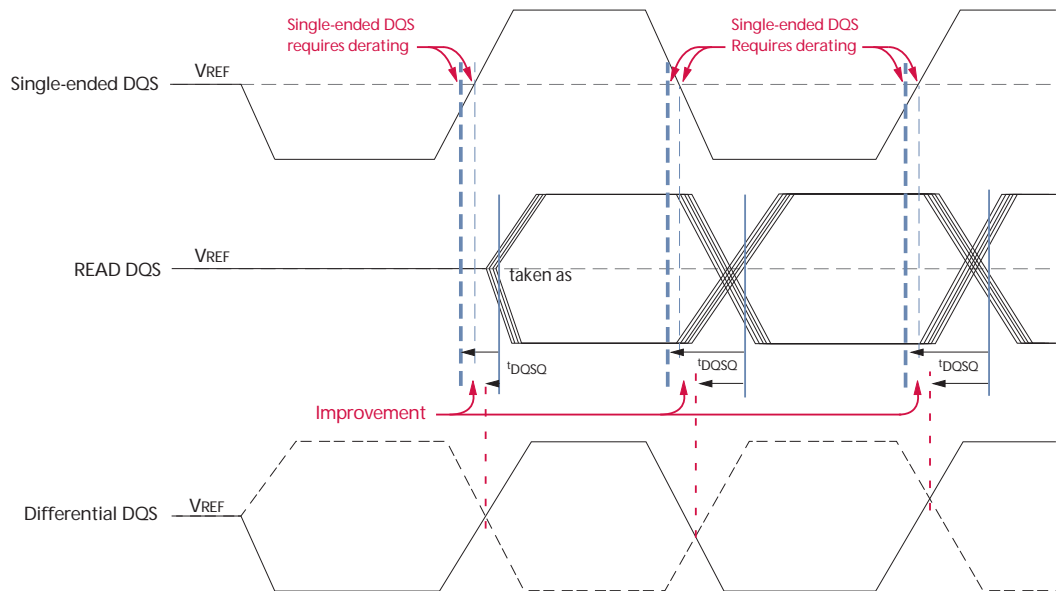
Tightly Controlled t_{DQSQ} (DQS-DQ Skew)

t_{DQSQ} performance can be improved using differential DQS signaling. This provides more margin to the specification value and requires less derating (see Figure 3 on page 4).

DQS reference timing points are the crossing points of the DQS and DQS# signals. Thus, differential DQS has one reference point, and single-ended DQS has two reference points (one is the crossing point of the rising DQS at V_{REF} , and the other is the falling DQS at V_{REF}). Therefore, one of the two crossing points will be larger (absolute value) than that of the differential DQS case, and the other will be smaller. The larger value is taken as t_{DQSQ} . Very seldom will the values of both the rising and falling edges be the same.

Differential signals can also minimize the effect of SSO on t_{DQSQ} . Because SSO depends on the DQ output switching combinations and because the crossing point of DQS and DQS# signals always exist between the crossing point of DQS/ V_{REF} and the crossing point of DQS#/ V_{REF} , the SSO effects are less than with single-ended DQS.

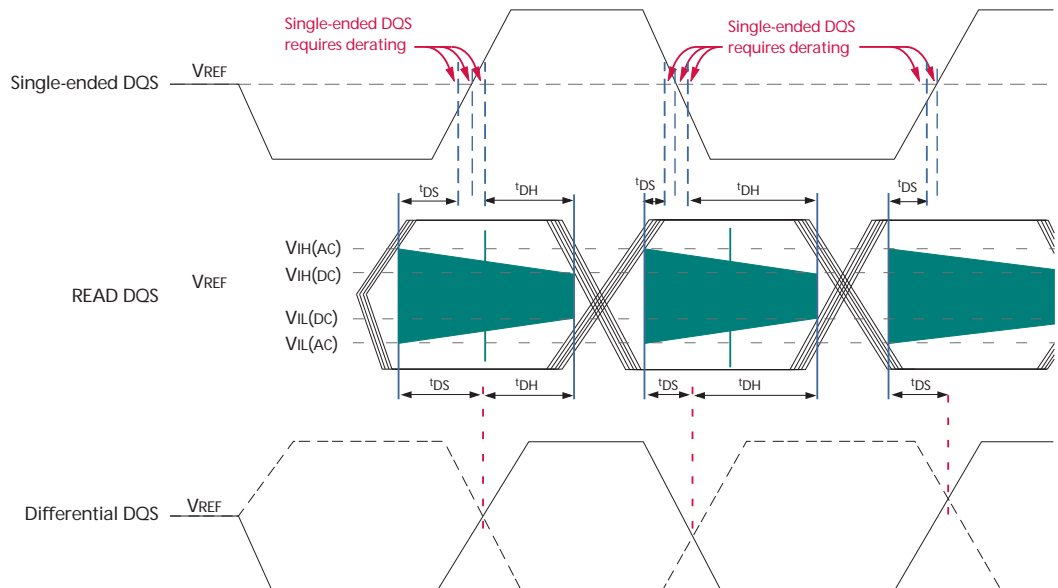
Figure 3: Single-Ended vs. Differential DQS Reference



t_{DS}/t_{DH} Specifications

t_{DS} (data input setup time) and t_{DH} (data input hold time) have two reference points with single-ended DQS. One is DQS rising at the V_{REF} crossing point and the other is DQS falling at the V_{REF} crossing point. t_{DS} and t_{DH} have to meet for both reference points. With differential DQS, only one reference point (the crossing point of DQS and DQS# input signals) is required for t_{DS} and t_{DH} (see Figure 4).

Figure 4: Single-Ended vs. Differential DQS for t_{DS}/t_{DH}



Conclusion

Enabling the differential DQS signaling in DDR2 devices can improve the accuracy in data capture timing across voltage and temperature fluctuations in the system.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmtg@micron.com www.micron.com Customer Comment Line: 800-932-4992

Micron, the M logo, and the Micron logo are trademarks of Micron Technology, Inc. All other trademarks are the property of their respective owners.