

Technical Note

NAND Flash Performance Increase

Using the Micron[®] PAGE READ CACHE MODE Command

For detailed product information, see the 2Gb NAND Flash data sheet at www.micron.com/products/nand/partlist.aspx.

Overview

NAND Flash devices are designed for applications requiring nonvolatile, high-density, solid-state storage. While NAND Flash provides sufficient speed for traditional applications, newer applications require higher data processing rates.

Typical programming time for current NAND Flash devices is 300 μ s for a 2KB page of data. Most NAND Flash devices have implemented a cache programming mechanism to accelerate Flash programming. Cache programming works by inputting a page (2KB) of data to the cache register, then transferring this data to the data register when the cache programming command is issued. At this point, the cache register is available to receive new data input while the data register simultaneously programs the Flash array.

In addition to cache programming operation, Micron has added PAGE READ CACHE MODE operation to further improve NAND Flash device performance. The PAGE READ CACHE MODE operation also uses the cache register; however, in this case, a page of data is transferred from the Flash array to the data register, then moved to the cache register when the PAGE READ CACHE MODE command is issued. After this command is issued, data can be clocked out of the cache register through the NAND Flash interface while the next page of data is simultaneously moved from the Flash array to the data register.

Overlapping the READ operation with data output can significantly improve data throughput, as shown in Figure 4 on page 8 and Figure 5 on page 9.

PAGE READ Operation

There are 2 COMMAND LATCH cycles and 5 ADDRESS LATCH cycles in a typical PAGE READ from a NAND Flash device. Following the ADDRESS LATCH cycles, R/B# goes LOW for t_R (a maximum of 25 μ s). PAGE READ operation details are provided in Tables 1 and 2 on page 3.

When R/B# is ready, data can be read sequentially, 1 byte per cycle. Assuming 50ns cycles, the time to read a page is calculated as follows:

$$\begin{aligned}
 \text{PAGE READ time} &= (2 \times t_{RC}) + (5 \times t_{RC}) + t_R + (\text{page size} \times t_{RC}) \\
 &= (2 \times 50\text{ns}) + (5 \times 50\text{ns}) + 25\mu\text{s} + (2,112 \times 50\text{ns}) \\
 &= 130.95\mu\text{s per page}
 \end{aligned}$$

Figure 1: Typical NAND Flash READ Operation Timing

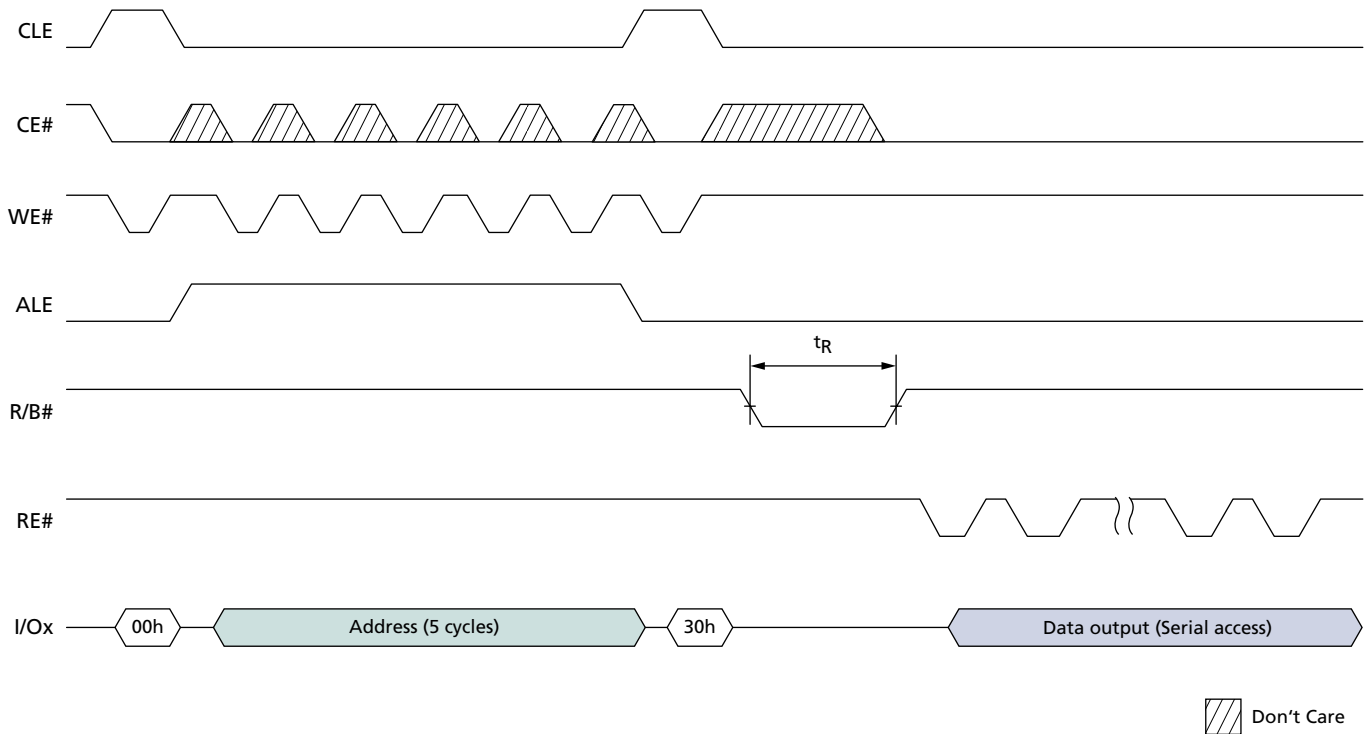




Table 1: Single-Block PAGE READ Operation Timing (x8)

Process	Repetitions	30ns Cycle Time		Unit
		Time	Total Time	
COMMAND LATCH (00h)	1	30	30	ns
ADDRESS LATCH	5	30	150	ns
COMMAND LATCH (30h)	1	30	30	ns
R/B# LOW (^t R)	1	25	25	μs
Data READ cycles	2,112	30		ns
Data READ cycles total page			63.36	μs
Total time to read a page			88.57	μs
Total time to read a block	64	0.08857	5.67	ms

Table 2: Single-Block PAGE READ Operation Timing (x16)

Process	Repetitions	50ns Cycle Time		Unit
		Time	Total Time	
COMMAND LATCH (00h)	1	50	50	ns
ADDRESS LATCH	5	50	250	ns
COMMAND LATCH (30h)	1	50	50	ns
R/B# LOW (^t R)	1	25	25	μs
Data READ cycles	1,056	50		ns
Data READ cycles total			52.8	μs
Total time to read a page			78.15	μs
Total time to read a block	64	0.07815	5.00	ms

PAGE READ CACHE MODE Operation

A PAGE READ CACHE MODE operation is started the same as a standard READ operation, by issuing the PAGE READ command (00h-30h). Assuming that a page 0 address is issued in the PAGE READ command, page 0 is copied from the memory array into the data register during this operation, and R/B# returns HIGH (25µs MAX) when the process is complete. The PAGE READ CACHE MODE command (31h) is used to transfer the page 0 data from the data register to the cache register and initiate a concurrent READ of the page 1 data from the memory array. R/B# will be LOW for a maximum of 3.0µs, after which data can be read from the cache register using data READ cycles.

After the page 0 READ from the cache register is completed, a new PAGE READ CACHE MODE command (31h) is issued to transfer the page 1 data from the data register to the cache register while simultaneously starting the transfer of page 2 data from the memory array into the data register. Sequential pages are read by issuing additional 31h commands.

To read the last page of data, PAGE READ CACHE MODE START LAST command (3Fh) is used. This command transfers data from the data register to the cache register without initiating a new memory read. It leaves the device ready for a new command immediately, even if the last page has been only partially read out of the cache register. Table 3, and Figure 2 on page 5 provide the signal and timing information required for PAGE READ CACHE MODE operations.

Tables 4 and 5 on page 6 show x8 and x16 timing calculations for READ clock cycles using PAGE READ CACHE MODE operations. As shown in Figure 4 on page 8, and Figure 5 on page 9, PAGE READ CACHE MODE does not provide a benefit for reading a single page; however, when two or more pages are read using PAGE READ CACHE MODE, performance gains are significant. When all 64 pages of a block are read using PAGE READ CACHE MODE, users realize a 33 percent READ performance increase over a regular PAGE READ on x8 devices running 50ns READ cycles, and a 39 percent READ performance increase on x16 devices running 50ns READ cycles.

Although these performance examples show only PAGE READ CACHE MODE used within a block, PAGE READ CACHE MODE can also be used across block boundaries.

Figure 3 on page 7 illustrates the PAGE READ CACHE MODE time savings.

Table 3: Worst-Case Timing Delays

Parameter	Description	Min	Max	Unit
^t R	Data transfer from Flash array to data register	–	25	µs
^t DCBSYR1	Cache busy in PAGE READ CACHE MODE operation (first 31h)	–	3.0	µs
^t DCBSYR2	Cache busy in PAGE READ CACHE MODE operation (next 31h and 3Fh)	^t DCBSYR1	25	µs

Figure 2: PAGE READ CACHE MODE Operation Timing

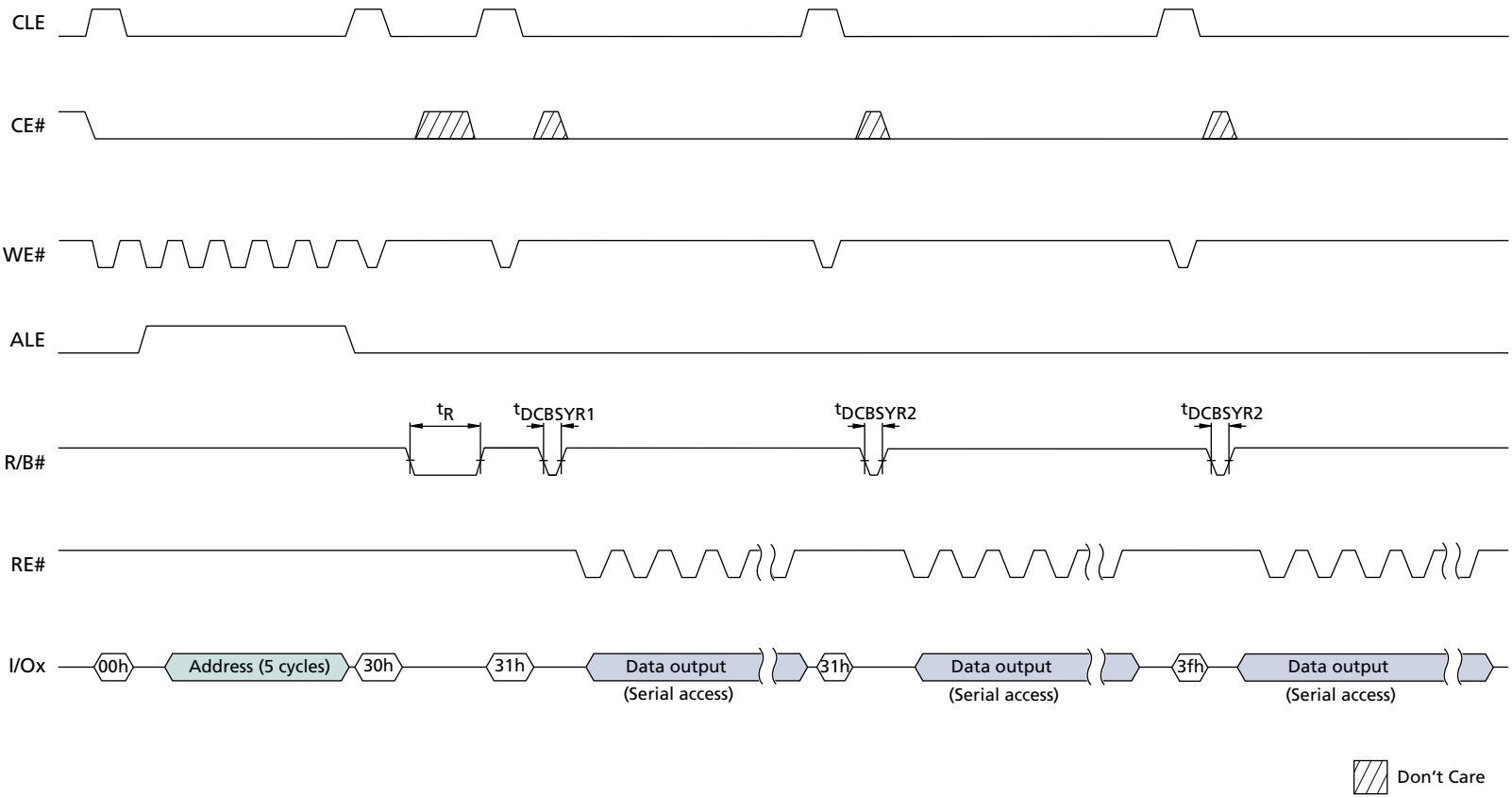




Table 4: Single-Block PAGE READ CACHE MODE Operation Timing (x8)

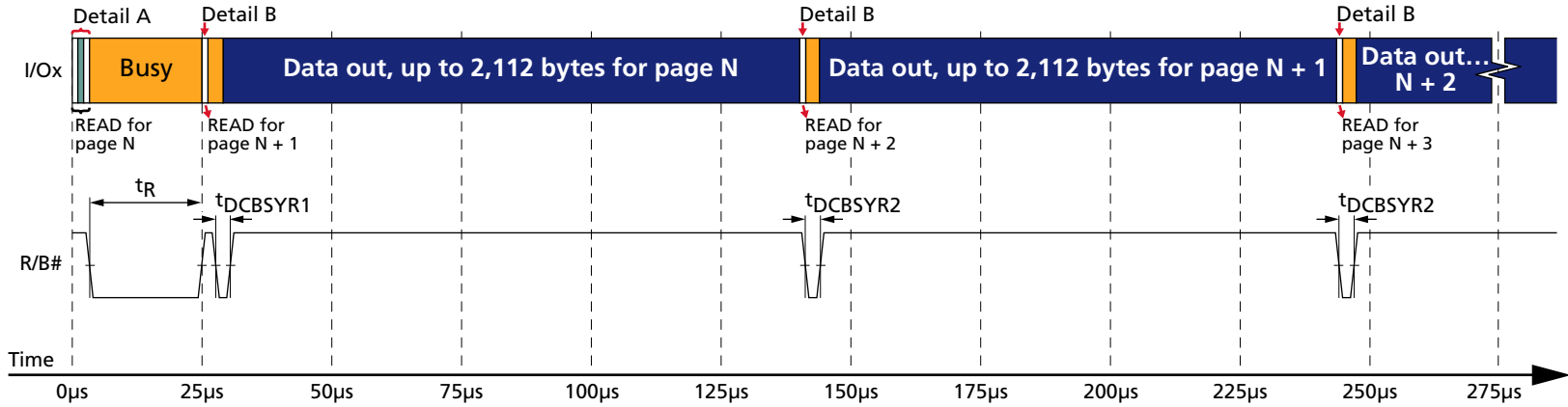
Process	Repetitions	30ns Cycle Time		Unit
		Time	Total Time	
COMMAND LATCH (00h)	1	30	30	ns
ADDRESS LATCH	5	30	150	ns
COMMAND LATCH (30h)	1	30	30	ns
R/B# LOW (^t R)	1	25	25	μs
COMMAND LATCH (31h)	1	30	30	ns
R/B# LOW (^t DCBSYR1)	1	3	3	μs
Data READ cycles	2,112	30		ns
Data READ cycles total			63.36	μs
Time to read page 0			91.6	μs
COMMAND LATCH (31h)	1	30	30	ns
R/B# LOW (^t DCBSYR2)	1	3	3	μs
Data READ (^t RC)	2,112	30	63.36	μs
Time to read page 1			66.39	μs
Time to read pages 2:63	62	0.06639	4.116	ms
Total time to read a block			4.274	ms

Table 5: Single-Block PAGE READ CACHE MODE Operation Timing (x16)

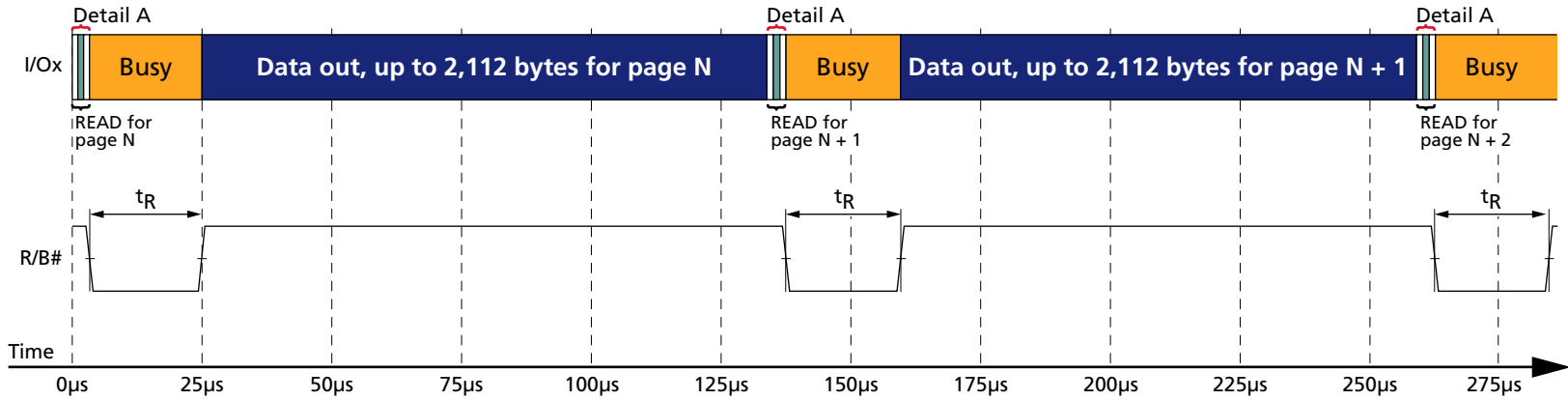
Process	Number of Cycles	50ns Cycle Time		Units
		Time/Cycle	Total Time	
Timing for page 0 READ				
COMMAND LATCH (00h)	1	50	50	ns
ADDRESS LATCH	5	50	250	ns
COMMAND LATCH (30h)	1	50	50	ns
R/B# LOW (^t R)	1	25	25	μs
COMMAND LATCH (31h)	1	50	50	ns
R/B# LOW (^t DCBSYR1)	1	3.0	3.0	μs
Data READ cycles	1,056	50		ns
Data READ cycles total page			52.8	μs
Time to read page 0			80.7	μs
COMMAND LATCH (31h)	1	50	50	ns
R/B# LOW (^t DCBSYR2)	1	3.0	3.0	μs
Data READ (^t RC)	1,056	50	52.8	μs
Time to read page 1			55.85	μs
Time to read pages 2:63	62	0.05585	3.463	ms
Total time to read a block			3.600	ms

Figure 3: Cache Read Time Savings Illustration

PAGE READ CACHE MODE Operation



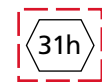
PAGE READ Operation



Detail A



Detail B

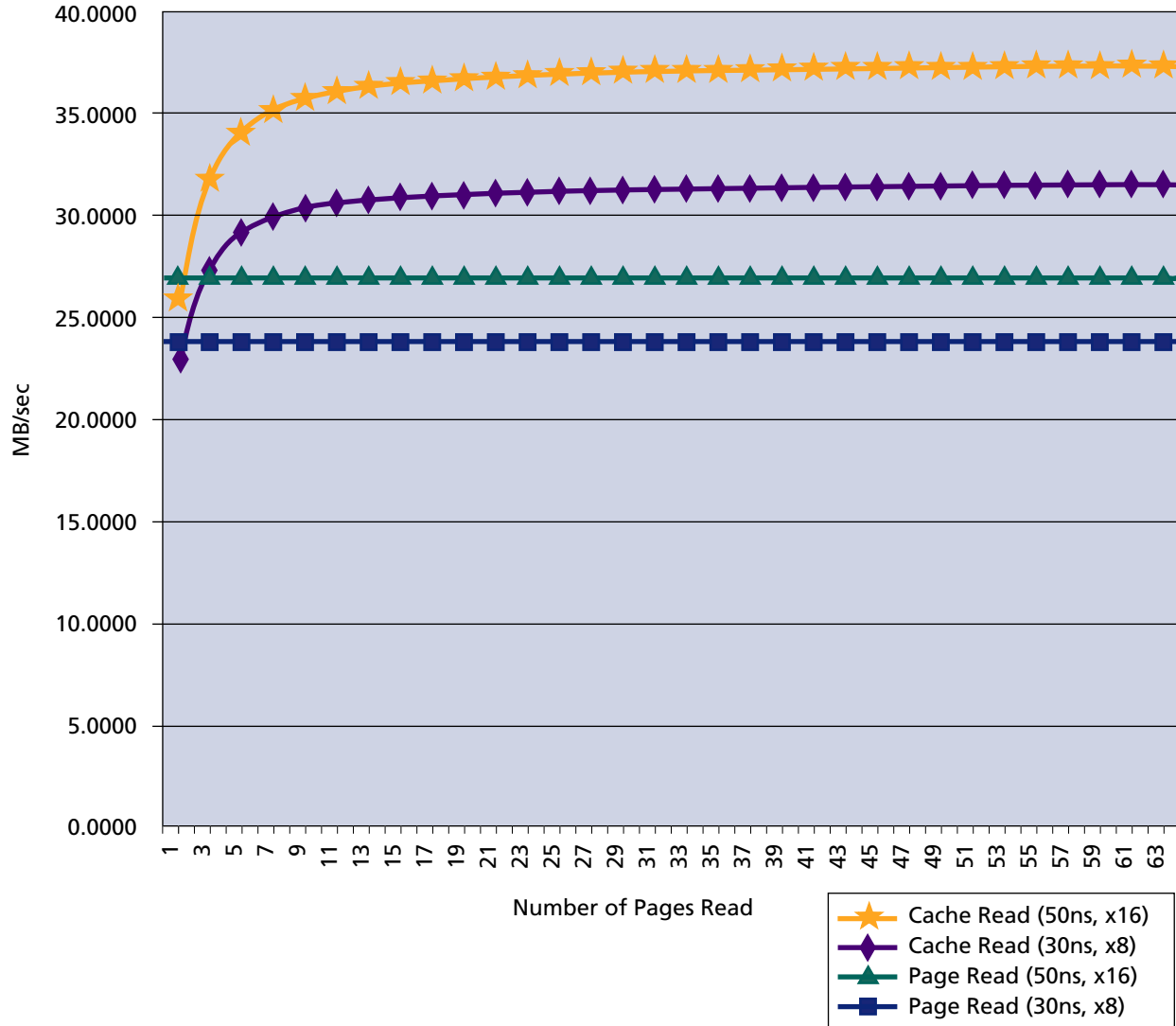


□ Commands ■ Address cycles ■ Busy ■ Data

Read Modes Comparison

Figure 4 illustrates speed gains in megabytes per second for each read mode. Performance gains are significant using cache mode READ operations.

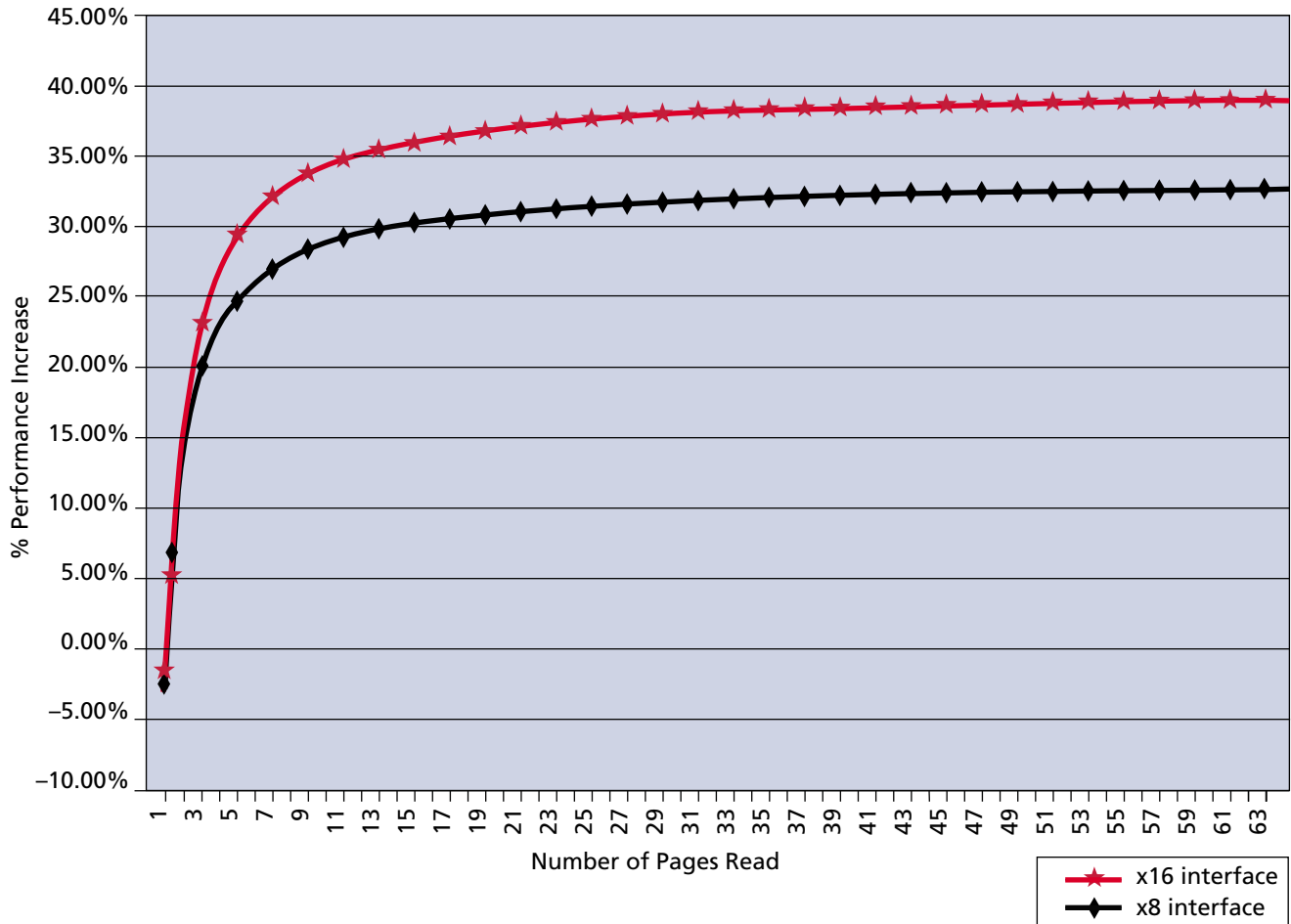
Figure 4: Speed Comparison: Cache Read Mode vs. Page Read Mode



Performance Increases

Figure 5 shows performance change percentages relative to the number of consecutive pages read. As the number of consecutive pages read increases, the performance gain increases. This is an asymptotic graph with the horizontal asymptote just above a 33 percent performance increase for x8 devices and a 39 percent performance increase for x16 devices.

Figure 5: READ Performance Increase Using PAGE READ CACHE MODE



Summary

Customers using the PAGE READ CACHE MODE operation provided in Micron NAND Flash devices will realize significant performance gains in systems requiring increased data volume at a much faster rate.



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Revision History

Rev. E	5/07
<ul style="list-style-type: none">• “Overview” on page 1: Revised description.• “PAGE READ Operation” on page 2: Revised heading and description.• Tables 1 and 2 on page 3: Moved to follow Figure 1 on page 2.• “PAGE READ CACHE MODE Operation” on page 4: Revised description.• Figure 3 on page 7: Replaced figure.• “Read Modes Comparison” on page 8: Revised heading.• “Performance Increases” on page 9: Changed 21 percent x8 performance increase to 33 percent.	
Rev. D	12/05
<ul style="list-style-type: none">• Figure 3 on page 7: Updated figure.	
Rev. C	11/05
<ul style="list-style-type: none">• Figure 3 on page 7: Updated figure.	
Rev. B	10/05
<ul style="list-style-type: none">• Table 1 on page 3 and Table 4 on page 6: Updated tables.• Figure 4 on page 8 and Figure 5 on page 9: Updated figures.	
Rev. A	4/05
<ul style="list-style-type: none">• Initial release.	