

Technical Note

Monitoring Ready/Busy Status in 2Gb, 4Gb, and 8Gb Micron NAND Flash Devices

For detailed NAND Flash device information, refer to www.micron.com/products/nand/.

Introduction

Systems that utilize NAND Flash memory can use either the ready/busy pin or the status register to determine if a Micron NAND Flash device is busy or ready to accept a new command. This technical note addresses only the use of status register bit 5, which indicates the ready/busy status of the NAND Flash device. In addition to the ready/busy status recommendations provided here, Micron also recommends making full use of status register bits 0 and 1 to check PROGRAM and ERASE success, bit 6 to check the cache ready/busy status, and bit 7 to check write protect status.

Four options for determining the NAND Flash ready/busy device status are presented in this technical note. Detailed explanations of each option follow.

Monitoring Ready/Busy Status Using the R/B# Pin

Micron NAND Flash devices are equipped with a ready/busy (R/B#) pin. The system can simply monitor this pin to determine the ready/busy status of the device. If the device is ready to accept a new command, R/B# will be HIGH; if the device is busy, R/B# will be LOW. This is the simplest method for determining the ready/busy status of the device; however, some systems lack the hardware resources to support the R/B# pin. In this case, other methods for monitoring NAND Flash device status are required.

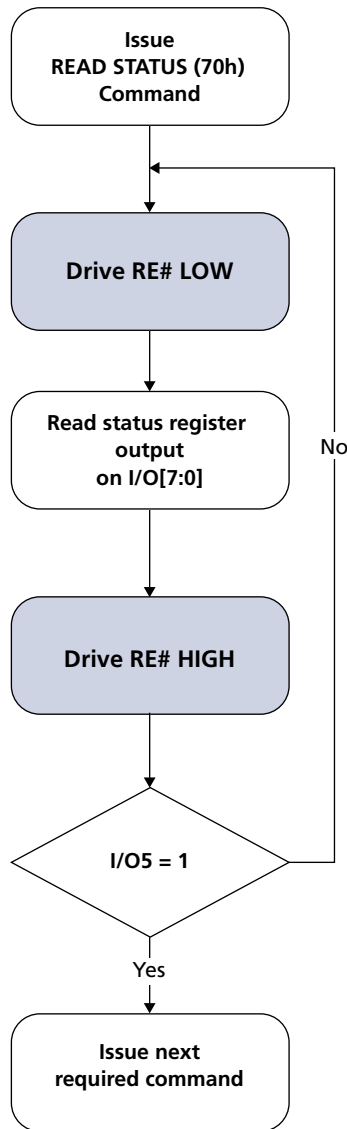
Monitoring Ready/Busy Using the READ STATUS (70h) Command

Micron NAND Flash devices are equipped with an 8-bit status register that the system software can read during device operation. When bit 5 of this status register is HIGH, the device is ready; when LOW, the device is busy. To access the status register, the system must issue the 70h command, then toggle the read enable (RE#) pin from HIGH to LOW. Additional considerations must be taken into account when the system reads status on a continuing basis. The following examples illustrate three different methods of monitoring ready/busy using the READ STATUS command.

READ STATUS Method 1

To use this method, issue the 70h command, drive the RE# pin LOW, and then drive it HIGH. The status register is output to the I/Os. If I/O5 is LOW, the NAND Flash device is busy; the system toggles RE# again and rechecks I/O5. This process continues until I/O5 = 1, indicating the NAND Flash device is ready for another command.

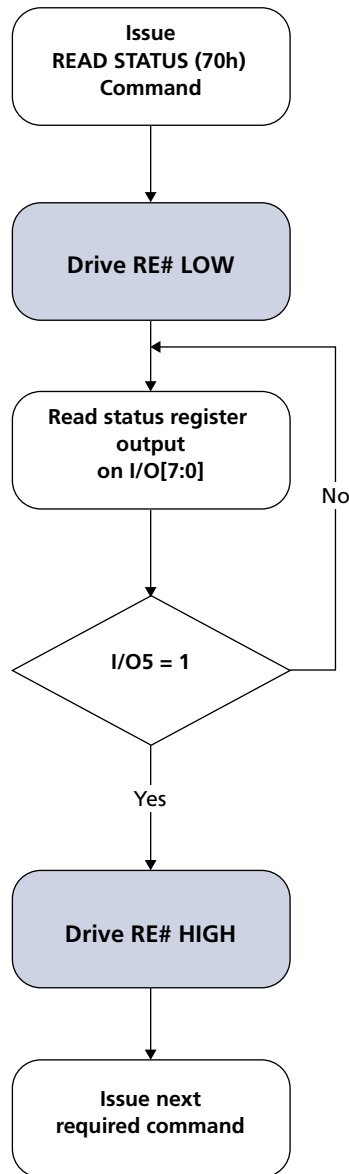
Figure 1: READ STATUS Method 1 Flow Chart



READ STATUS Method 2

To use this method, issue the 70h command and hold the RE# pin LOW. The status register output will continually change on the I/Os when RE# is LOW, so the user can simply monitor the output on I/O5 and wait for it to go HIGH, after which the next command can be issued.

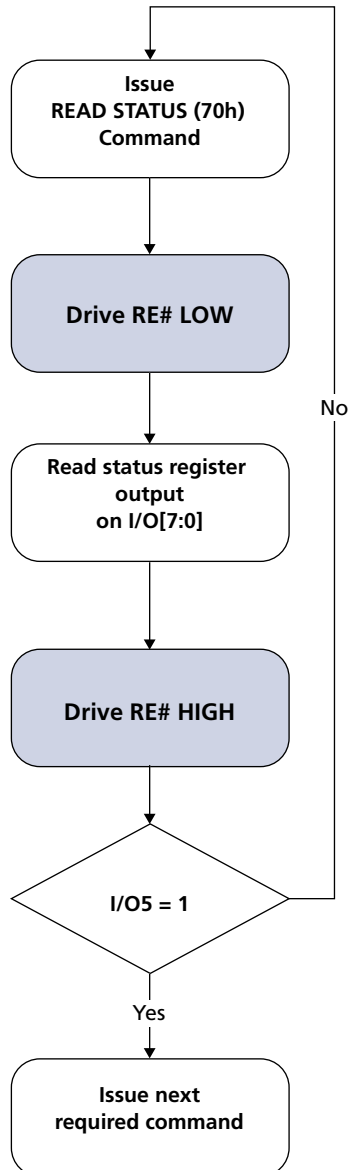
Figure 2: READ STATUS Method 2 Flow Chart



READ STATUS Method 3 (Not supported)

To use this method, issue the 70h command, drive the RE# pin LOW, and then drive it HIGH. The status register is output to the I/Os. If I/O5 is LOW, the NAND Flash device is busy; the system issues another 70h command, then toggles RE# again and rechecks I/O5. This process continues until I/O5 = 1, indicating that the NAND Flash device is ready for another command.

Figure 3: READ STATUS Method 3 Flow Chart



Recommendations

Micron recommends monitoring the ready/busy status of NAND Flash devices using the R/B# pin, as this is the simplest method and requires the least software interaction between the system and the NAND Flash device.

Where a system lacks hardware resources to support the R/B# pin, Micron recommends using READ STATUS Method 1 or 2. These methods require fewer system resources than READ STATUS Method 3.



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Revision History

Rev. B 5/07

- Page 1: Updated Web link and revised description.
- “READ STATUS Method 3 (Not supported)” on page 4: Revised description.
- Former Table 1 on page 5: Deleted table.
- “Recommendations” on page 5: Revised description.

Rev. A 10/05

- Initial release.