

# Technical Note

## **Improving NAND Flash Performance Using Two-Plane Command Enabled Micron® Devices MT29F4G08AAA, MT29F8G08BAA, MT29F8G08DAA, MT29F16G08FAA, MT29F8G08MAA, MT29F16G08QAA, and MT29F32G08TAA**

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### Introduction

NAND Flash devices have found a strong foothold as a viable solution for solid-state mass storage, both as a removable storage medium and as an embedded storage medium. The number of NAND Flash implementations has increased steadily, and basic understanding of first-generation NAND Flash commands has also increased. The newest Micron® two-plane NAND Flash devices now offer a command superset that builds on the original command set to deliver the improved READ, PROGRAM, and ERASE performance the market demands.

Micron two-plane NAND Flash devices support simultaneous PROGRAM and READ operations to two pages, or simultaneous ERASE operations to two blocks, with minimal added command and address overhead. These two-plane commands increase PROGRAM, READ, and ERASE performance in all Micron two-plane NAND Flash devices.

This technical note describes the performance benefits of Micron two-plane commands, and provides implementation guidelines for making the best use of two-plane capabilities.



## Two-Plane Commands for Micron NAND Flash Devices

The Micron two-plane command set is a superset of the standard NAND Flash command set, making Micron two-plane NAND Flash devices fully backward compatible with previous Micron NAND Flash devices. The command superset includes two-plane equivalent commands for READ, PROGRAM, INTERNAL DATA MOVE, and ERASE operations. Table 1 shows Micron standard NAND Flash commands and corresponding Micron two-plane commands.

**Table 1: NAND Flash Command Set Comparison**

| Standard Micron NAND Flash Commands |         | Two-Plane Micron NAND Flash Commands     |                 |
|-------------------------------------|---------|--|-----------------|
| Command Name                        | Opcodes | Command Name                             | Opcodes         |
| PAGE READ                           | 00h-30h | TWO-PLANE PAGE READ                      | 00h-00h-30h     |
| RANDOM DATA READ                    | 05h-E0h | TWO-PLANE RANDOM DATA READ               | 06h-E0h         |
| READ for INTERNAL DATA MOVE         | 00h-35h | TWO-PLANE READ for INTERNAL DATA MOVE    | 00h-00h-35h     |
| PROGRAM PAGE                        | 80h-10h | TWO-PLANE PROGRAM PAGE                   | 80h-11h-80h-10h |
| PROGRAM PAGE CACHE MODE             | 80h-15h | TWO-PLANE PROGRAM PAGE CACHE MODE        | 80h-11h-80h-15h |
| PROGRAM for INTERNAL DATA MOVE      | 85h-10h | TWO-PLANE PROGRAM for INTERNAL DATA MOVE | 85h-11h-80h-10h |
| BLOCK ERASE                         | 60h-D0h | TWO-PLANE BLOCK ERASE                    | 60h-60h-D0h     |

Details and timing diagrams for NAND Flash two-plane commands can be found in the data sheets for two-plane Micron NAND Flash devices, at [www.micron.com/products/nand/](http://www.micron.com/products/nand/).

### Benefits of Micron Two-Plane Commands

The most efficient approach for increasing NAND Flash READ, PROGRAM, and ERASE performance—with minimal effort—is to implement the Micron two-plane commands. This is particularly advantageous for multilevel cell (MLC) NAND Flash devices. Array operations on MLC devices are typically slower than their single-level cell (SLC) counterparts, and the two-plane commands can improve MLC performance.

Two-plane commands can also be used for interleaved die operations to further increase READ, PROGRAM, and ERASE performance in Micron NAND Flash devices that support these commands. To determine which two-plane commands can be used during interleaved die operations, see the Micron NAND Flash data sheet for the device used.

Tables 2 through 6 on the following pages compare raw NAND Flash performance in READ, PROGRAM and ERASE operations using Micron standard and two-plane commands. In each instance, the performance gain using two-plane commands is significant.

### TWO-PLANE PAGE READ Performance

Although READ throughput has not generally been considered a bottleneck for NAND Flash performance, it is becoming more important as NAND Flash is employed in video and other high-resolution mass data storage environments. These applications typically require high-speed read-out from the NAND Flash device.

The TWO-PLANE PAGE READ (00h-00h-30h) command improves performance by reading two pages simultaneously from the NAND Flash device. This is much faster than using a standard sequential PAGE READ (00h-30h) command.

Raw performance timings are shown in Table 2 on page 4. This table compares standard PAGE READ timing with TWO-PLANE PAGE READ timing using Micron two-plane SLC and MLC NAND Flash devices.



## TN-29-25: Improving Performance Using Two-Plane Commands Benefits of Micron Two-Plane Commands

**Table 2: PAGE READ 00h-30h vs. TWO-PLANE PAGE READ 00h-00h-30h**

| Process  | Repetitions |     | 25ns Min Cycle Time |               |               |               | READ Performance      |                       |
|--|-------------|-----|---------------------|---------------|---------------|---------------|-----------------------|-----------------------|
|  |             |     | Time per Cycle      |               | Total Time    |               |                       |                       |
|  | SLC         | MLC | SLC                 | MLC           | SLC           | MLC           | SLC                   | MLC                   |
| <b>PAGE READ 00h-30h<sup>1</sup></b>               |             |     |                     |               |               |               |                       |                       |
| Command latch (00h)                                | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| Address latch                                      | 5           |     | 25ns                |               | 125ns         |               |                       |                       |
| Command latch (30h or 35h)                         | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| R/B# LOW ( <sup>†</sup> R)                         | 1           |     | 20µs<br>(MAX)       | 50µs<br>(MAX) | 20µs<br>(MAX) | 50µs<br>(MAX) |                       |                       |
| Read data cycles (page size)                       | 2,112       |     | 25ns                |               | 52.8µs        |               |                       |                       |
| Total time to read a page                          |             |     |                     |               | 72.975µs      | 102.975µs     |                       |                       |
| Total time to read a block<br>(pages per block)    | 64          | 128 |                     |               | 4.67ms        | 13.18ms       |                       |                       |
| READ performance<br>(1,024 kilobytes per MB)       |             |     |                     |               |               |               | <b>28.94<br/>MB/s</b> | <b>20.51<br/>MB/s</b> |
| <b>TWO-PLANE PAGE READ 00h-00h-30h<sup>2</sup></b> |             |     |                     |               |               |               |                       |                       |
| Command latch (00h)                                | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| Address latch                                      | 5           |     | 25ns                |               | 125ns         |               |                       |                       |
| Command latch (00h)                                | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| Address latch                                      | 5           |     | 25ns                |               | 125ns         |               |                       |                       |
| Command latch (30h or 35h)                         | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| R/B# LOW ( <sup>†</sup> R)                         | 1           |     | 20µs<br>(MAX)       | 50µs<br>(MAX) | 20µs<br>(MAX) | 50µs<br>(MAX) |                       |                       |
| Read data cycles<br>(page size, 1st plane)         | 2,112       |     | 25ns                |               | 52.8µs        |               |                       |                       |
| Command latch (06h)                                | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| Address latch                                      | 5           |     | 25ns                |               | 125ns         |               |                       |                       |
| Command latch (E0h)                                | 1           |     | 25ns                |               | 25ns          |               |                       |                       |
| Read data cycles<br>(page size, 2nd plane)         | 2,112       |     | 25ns                |               | 52.8µs        |               |                       |                       |
| Total time to read 2 pages                         |             |     |                     |               | 106.12µs      | 156.1µs       |                       |                       |
| Total time to read 2 blocks<br>(pages per block)   | 64          | 128 |                     |               | 6.79ms        | 19.98ms       |                       |                       |
| READ performance<br>(1,024 kilobytes per MB)       |             |     |                     |               |               |               | <b>37.97<br/>MB/s</b> | <b>25.81<br/>MB/s</b> |

- Notes:
1. Results for the PAGE READ (00h-30h) command are identical for the READ for INTERNAL DATA MOVE (00h-35h) command.
  2. Results for the TWO-PLANE PAGE READ (00h-00h-30h) command are identical for the TWO-PLANE READ for INTERNAL DATA MOVE (00h-00h-35h) command.

With the TWO-PLANE PAGE READ command, read throughput is approximately 31 percent higher than standard PAGE READ throughput for SLC NAND Flash devices and approximately 26 percent higher for MLC devices.



**TWO-PLANE PROGRAM PAGE Performance**

Programming performance has long been a primary consideration when determining the most suitable applications for NAND Flash devices. TWO-PLANE PROGRAM PAGE commands deliver marked performance increases in programming throughput. Micron NAND Flash devices capable of two-plane operations offer cost and performance advantages over other devices.

The TWO-PLANE PROGRAM PAGE (80h-11h-80h-10h) command supports simultaneous two-page programming that surpasses standard PROGRAM PAGE (80h-10h) performance.

Raw performance timings are shown in Table 3. This table compares standard PROGRAM PAGE timing with TWO-PLANE PROGRAM PAGE timing using Micron two-plane SLC and MLC NAND Flash devices.

**Table 3: PROGRAM PAGE 80h-10h vs. TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h**

| Process  | Repetitions |     | 25ns Min Cycle Time |             |             |             | PROGRAM Performance |                  |
|--|-------------|-----|---------------------|-------------|-------------|-------------|---------------------|------------------|
|  |             |     | Time per Cycle      |             | Total Time  |             |                     |                  |
|  | SLC         | MLC | SLC                 | MLC         | SLC         | MLC         | SLC                 | MLC              |
| <b>PROGRAM PAGE 80h-10h</b>                      |             |     |                     |             |             |             |                     |                  |
| Command latch (80h)                              | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| Address latch                                    | 5           |     | 25ns                |             | 125ns       |             |                     |                  |
| Program data cycles (page size)                  | 2,112       |     | 25ns                |             | 52.8µs      |             |                     |                  |
| Command latch (10h)                              | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| R/B# LOW ( <sup>t</sup> PROG)                    | 1           |     | 220µs (TYP)         | 650µs (TYP) | 220µs (TYP) | 650µs (TYP) |                     |                  |
| Total time to program a page                     |             |     |                     |             | 272.98µs    | 702.98µs    |                     |                  |
| Total time to program a block (pages per block)  | 64          | 128 |                     |             | 17.47ms     | 89.98ms     |                     |                  |
| PROGRAM performance (1,024 kilobytes per MB)     |             |     |                     |             |             |             | <b>7.38 MB/s</b>    | <b>2.87 MB/s</b> |
| <b>TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h</b>    |             |     |                     |             |             |             |                     |                  |
| Command latch (80h)                              | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| Address latch                                    | 5           |     | 25ns                |             | 125ns       |             |                     |                  |
| Program data cycles (page size, 1st plane)       | 2,112       |     | 25ns                |             | 52.8µs      |             |                     |                  |
| Command latch (11h)                              | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| R/B# LOW ( <sup>t</sup> DBSY)                    | 1           |     | 1µs                 |             | 1µs         |             |                     |                  |
| Command latch (80h)                              | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| Address latch                                    | 5           |     | 25ns                |             | 125ns       |             |                     |                  |
| Program data cycles (page size, 2nd plane)       | 2,112       |     | 25ns                |             | 52.8µs      |             |                     |                  |
| Command latch (10h)                              | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| R/B# LOW ( <sup>t</sup> PROG)                    | 1           |     | 220µs (TYP)         | 650µs (TYP) | 220µs (TYP) | 650µs (TYP) |                     |                  |
| Total time to program 2 pages                    |             |     |                     |             | 326.95µs    | 756.95µs    |                     |                  |
| Total time to program 2 blocks (pages per block) | 64          | 128 |                     |             | 20.92ms     | 96.89ms     |                     |                  |
| PROGRAM performance (1,024 kilobytes per MB)     |             |     |                     |             |             |             | <b>12.32 MB/s</b>   | <b>5.32 MB/s</b> |



## TN-29-25: Improving Performance Using Two-Plane Commands Benefits of Micron Two-Plane Commands

With the TWO-PLANE PROGRAM PAGE command, programming throughput is approximately 67 percent higher than standard PROGRAM PAGE throughput for an SLC NAND Flash device and approximately 85 percent higher for an MLC device.

### TWO-PLANE PROGRAM PAGE CACHE MODE Performance

Similar to the TWO-PLANE PROGRAM PAGE command, the TWO-PLANE PROGRAM PAGE CACHE MODE command offers two-plane programming with the addition of cache functionality to further increase programming performance. TWO-PLANE PROGRAM PAGE CACHE MODE performance surpasses standard PROGRAM PAGE CACHE MODE performance.

Raw performance timings for cache mode programming are shown in Table 4. This table compares standard PROGRAM PAGE CACHE MODE timing with TWO-PLANE PROGRAM PAGE CACHE MODE timing in Micron two-plane SLC and MLC NAND Flash devices.

**Table 4: PROGRAM PAGE CACHE MODE 80h-15h vs. TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h**

| Process  | Repetitions |     | 25ns Min Cycle Time |             |             |             | PROGRAM Performance |                  |
|--|-------------|-----|---------------------|-------------|-------------|-------------|---------------------|------------------|
|  |             |     | Time per Cycle      |             | Total Time  |             | SLC                 | MLC              |
|  | SLC         | MLC | SLC                 | MLC         | SLC         | MLC         |                     |                  |
| <b>PROGRAM PAGE CACHE MODE 80h-15h</b>                   |             |     |                     |             |             |             |                     |                  |
| Command latch (80h)                                      | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| Address latch  | 5           |     | 25ns                |             | 125ns       |             |                     |                  |
| Program data cycles (page size)                          | 2,112       |     | 25ns                |             | 52.8µs      |             |                     |                  |
| Command latch (15h)                                      | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| R/B# LOW (1st <sup>t</sup> CBSY)                         | 1           |     | 3µs                 | 7µs         | 3µs         | 7µs         |                     |                  |
| Time to program page 0                                   |             |     |                     |             | 55.98µs     | 59.975µs    |                     |                  |
| R/B# LOW ( <sup>t</sup> CBSY)                            | 62          | 126 | 220µs (TYP)         | 650µs (TYP) | 220µs (TYP) | 650µs (TYP) |                     |                  |
| Time to program page 1 to (last page - 1)                |             |     |                     |             | 13.64ms     | 81.90ms     |                     |                  |
| R/B# LOW ( <sup>t</sup> LPROG) for last page             | 1           |     |                     |             | 167.2µs     | 594.7µs     |                     |                  |
| Total time to program 1 block                            |             |     |                     |             | 13.86ms     | 82.55ms     |                     |                  |
| PROGRAM performance (1,024 kilobytes per MB)             |             |     |                     |             |             |             | <b>9.30 MB/s</b>    | <b>3.12 MB/s</b> |
| <b>TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h</b> |             |     |                     |             |             |             |                     |                  |
| Command latch (80h)                                      | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| Address latch  | 5           |     | 25ns                |             | 125ns       |             |                     |                  |
| Program data cycles (page size, 1st plane)               | 2,112       |     | 25ns                |             | 52.8µs      |             |                     |                  |
| Command latch (11h)                                      | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| R/B# LOW ( <sup>t</sup> DBSY)                            | 1           |     | 1µs                 |             | 1µs         |             |                     |                  |
| Command latch (80h)                                      | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| Address latch  | 5           |     | 25ns                |             | 125ns       |             |                     |                  |
| Program data cycles (page size, 2nd plane)               | 2,112       |     | 25ns                |             | 52.8µs      |             |                     |                  |
| Command latch (15h)                                      | 1           |     | 25ns                |             | 25ns        |             |                     |                  |
| R/B# LOW (1st <sup>t</sup> CBSY)                         | 1           |     | 3µs                 | 7µs         | 3µs         | 7µs         |                     |                  |

**Table 4: PROGRAM PAGE CACHE MODE 80h-15h vs. TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h (continued)**

| Process  | Repetitions |     | 25ns Min Cycle Time |             |             |             | PROGRAM Performance |                  |
|--|-------------|-----|---------------------|-------------|-------------|-------------|---------------------|------------------|
|  |             |     | Time per Cycle      |             | Total Time  |             |                     |                  |
|  | SLC         | MLC | SLC                 | MLC         | SLC         | MLC         | SLC                 | MLC              |
| Time to program page 0 for 1st and 2nd plane                                     |             |     |                     |             | 109.95µs    | 113.95µs    |                     |                  |
| R/B# LOW ( <sup>T</sup> DBSY) for page 1 to (last page - 1) on 1st and 2nd plane | 62          | 126 | 1µs                 |             | 1µs         |             |                     |                  |
| R/B# LOW ( <sup>T</sup> CBSY)  | 62          | 126 | 220µs (TYP)         | 650µs (TYP) | 220µs (TYP) | 650µs (TYP) |                     |                  |
| Time to program page 1 to (last page - 1) on 1st and 2nd plane                   |             |     |                     |             | 13.70ms     | 82.03ms     |                     |                  |
| R/B# LOW ( <sup>T</sup> DBSY) for last page on 1st and 2nd plane                 | 1           |     | 1µs                 |             | 1µs         |             |                     |                  |
| R/B# LOW ( <sup>T</sup> LPROG) for last page on 1st and 2nd plane                | 1           |     |                     |             | 167.2µs     | 594.7µs     |                     |                  |
| Total time to program 2 blocks   |             |     |                     |             | 13.98ms     | 82.74ms     |                     |                  |
| PROGRAM performance (1,024 kilobytes per MB)                                     |             |     |                     |             |             |             | <b>18.44 MB/s</b>   | <b>6.23 MB/s</b> |

With the TWO-PLANE PROGRAM PAGE CACHE MODE command, in both SLC and MLC devices, programming throughput is approximately 100 percent higher than throughput with the standard PROGRAM PAGE CACHE MODE command.

## TWO-PLANE PROGRAM for INTERNAL DATA MOVE Performance

During the normal course of data maintenance in the NAND Flash array, invalid data is erased and valid data is moved to new locations within the NAND Flash array. Many data maintenance operations occur as background tasks during idle periods. NAND Flash INTERNAL DATA MOVE operations are well suited for this type of data maintenance as they don't require data input cycles when moving data internally from one part of the NAND Flash array to another.

The TWO-PLANE PROGRAM for INTERNAL DATA MOVE (85h-11h-80h-10h) command supports simultaneous programming of two pages of the NAND Flash device. This is much more efficient than using the standard PROGRAM for INTERNAL DATA MOVE (85h-10h) command.

Raw performance timings are shown in Table 5. This table compares standard PROGRAM for INTERNAL DATA MOVE timing with TWO-PLANE PROGRAM for INTERNAL DATA MOVE timing using Micron two-plane SLC and MLC NAND Flash devices.



**Table 5: PROGRAM for INTERNAL DATA MOVE 85h-10h vs. TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-80h-10h**

| Process   | Repetitions |     | 25ns Min Cycle Time |             |             |             | PROGRAM for INTERNAL DATA MOVE Performance |                  |
|---|-------------|-----|---------------------|-------------|-------------|-------------|--|------------------|
|   |             |     | Time per Cycle      |             | Total Time  |             |  |                  |
|   | SLC         | MLC | SLC                 | MLC         | SLC         | MLC         | SLC  | MLC              |
| <b>PROGRAM for INTERNAL DATA MOVE 85h-10h</b>                   |             |     |                     |             |             |             |  |                  |
| Command latch (85h)   | 1           |     | 25ns                |             | 25ns        |             |  |                  |
| Address latch   | 5           |     | 25ns                |             | 125ns       |             |  |                  |
| Command latch (10h)   | 1           |     | 25ns                |             | 25ns        |             |  |                  |
| R/B# LOW ( <sup>†</sup> PROG)                                   | 1           |     | 220µs (TYP)         | 650µs (TYP) | 220µs (TYP) | 650µs (TYP) |  |                  |
| Total time to program a page                                    |             |     |                     |             | 220.125µs   | 650.125µs   |  |                  |
| Total time to program a block (pages per block)                 | 64          | 128 |                     |             | 14.10ms     | 83.22ms     |  |                  |
| PROGRAM performance (1,024 kilobytes per MB)                    |             |     |                     |             |             |             | <b>8.87 MB/s</b>                           | <b>3.00 MB/s</b> |
| <b>TWO-PLANE PROGRAM for INTERNAL DATA MOVE 85h-11h-80h-10h</b> |             |     |                     |             |             |             |  |                  |
| Command latch (85h)   | 1           |     | 25ns                |             | 25ns        |             |  |                  |
| Address latch   | 5           |     | 25ns                |             | 125ns       |             |  |                  |
| Command latch (11h)   | 1           |     | 25ns                |             | 25ns        |             |  |                  |
| R/B# LOW ( <sup>†</sup> DBSY)                                   | 1           |     | 1µs                 |             | 1µs         |             |  |                  |
| Command latch (80h)   | 1           |     | 25ns                |             | 25ns        |             |  |                  |
| Address latch   | 5           |     | 25ns                |             | 125ns       |             |  |                  |
| Command latch (10h)   | 1           |     | 25ns                |             | 25ns        |             |  |                  |
| R/B# LOW ( <sup>†</sup> PROG)                                   | 1           |     | 220µs (TYP)         | 650µs (TYP) | 220µs (TYP) | 650µs (TYP) |  |                  |
| Total time to program 2 pages                                   |             |     |                     |             | 221.35µs    | 651.35µs    |  |                  |
| Total time to program 2 blocks (pages per block)                | 64          | 128 |                     |             | 14.17ms     | 83.37ms     |  |                  |
| PROGRAM performance (1,024 kilobytes per MB)                    |             |     |                     |             |             |             | <b>17.64 MB/s</b>                          | <b>6.00 MB/s</b> |

With the TWO-PLANE PROGRAM for INTERNAL DATA MOVE command, in both SLC and MLC devices, programming throughput is approximately 100 percent higher than throughput with the standard PROGRAM for INTERNAL DATA MOVE command.

## TWO-PLANE BLOCK ERASE Performance

NAND Flash devices can only program bits from “1” to “0,” so it is important to have free NAND Flash blocks erased and ready for programming when they are needed. To avoid the delay of waiting for blocks to be erased before a programming operation can take place, applications typically perform BLOCK ERASE operations in the NAND Flash array during idle time, when no active READ or PROGRAM operations are taking place.

The TWO-PLANE BLOCK ERASE (60h-60h-D0h) command takes further advantage of idle time by simultaneously erasing two blocks of the NAND Flash device as opposed to the single block that would be erased using the standard BLOCK ERASE (60h-D0h) command.



## TN-29-25: Improving Performance Using Two-Plane Commands Requirements for Using Micron Two-Plane Commands

Raw erase performance timings are shown in Table 6. This table compares standard BLOCK ERASE timing with TWO-PLANE BLOCK ERASE timing in SLC and MLC NAND Flash devices.

**Table 6: BLOCK ERASE 60h-D0h vs. TWO-PLANE BLOCK ERASE 60h-60h-D0h**

| Process                                       | Repetitions |     | 25ns Min Cycle Time |              |                |              | ERASE Performance      |                        |
|---|-------------|-----|---------------------|--------------|----------------|--------------|------------------------|------------------------|
|   |             |     | Time per Cycle      |              | Total Time     |              |                        |                        |
|   | SLC         | MLC | SLC                 | MLC          | SLC            | MLC          | SLC                    | MLC                    |
| <b>BLOCK ERASE 60h-D0h</b>                    |             |     |                     |              |                |              |                        |                        |
| Command latch (60h)                           | 1           |     | 25ns                |              | 25ns           |              |                        |                        |
| Address latch                                 | 3           |     | 25ns                |              | 75ns           |              |                        |                        |
| Command latch (D0h)                           | 1           |     | 25ns                |              | 25ns           |              |                        |                        |
| R/B# LOW ( <sup>t</sup> BERS)                 | 1           |     | 1.5ms<br>(TYP)      | 2ms<br>(TYP) | 1.5ms<br>(TYP) | 2ms<br>(TYP) |                        |                        |
| Total time to erase 1 block                   |             |     |                     |              | 1.5ms          | 2ms          |                        |                        |
| ERASE performance<br>(1,024 kilobytes per MB) |             |     |                     |              |                |              | <b>85.94<br/>MB/s</b>  | <b>128.91<br/>MB/s</b> |
| <b>TWO-PLANE BLOCK ERASE 60h-60h-D0h</b>      |             |     |                     |              |                |              |                        |                        |
| Command latch (60h)                           | 1           |     | 25ns                |              | 25ns           |              |                        |                        |
| Address latch                                 | 3           |     | 25ns                |              | 75ns           |              |                        |                        |
| Command latch (60h)                           | 1           |     | 25ns                |              | 25ns           |              |                        |                        |
| Address latch                                 | 3           |     | 25ns                |              | 75ns           |              |                        |                        |
| Command latch (D0h)                           | 1           |     | 25ns                |              | 25ns           |              |                        |                        |
| R/B# LOW ( <sup>t</sup> BERS)                 | 1           |     | 1.5ms<br>(TYP)      | 2ms<br>(TYP) | 1.5ms<br>(TYP) | 2ms<br>(TYP) |                        |                        |
| Total time to erase 2 blocks                  |             |     |                     |              | 1.5ms          | 2ms          |                        |                        |
| ERASE performance<br>(1,024 kilobytes per MB) |             |     |                     |              |                |              | <b>171.84<br/>MB/s</b> | <b>257.81<br/>MB/s</b> |

With the TWO-PLANE BLOCK ERASE command, in both MLC and SLC NAND Flash devices, erase throughput is approximately 100 percent higher than that of the standard BLOCK ERASE command.

## Requirements for Using Micron Two-Plane Commands

Micron two-plane commands offer significant performance gains when the following implementation requirements are met:

- Two-plane commands can only be used within the same physical NAND Flash die. To determine die address boundaries, see the Micron NAND Flash data sheet for the device used.
- The least significant block address bit, BA6 for SLC devices and BA7 for MLC devices, must be different for each of the two NAND Flash addresses used in all two-plane commands.
- The page address bits, PA[5:0] for SLC devices and PA[6:0] for MLC devices, must be identical for both of the addresses used in two-plane commands that require page-address bits.

## Summary

While NAND Flash devices have continued to migrate to smaller technology production nodes, NAND Flash memory-array access times have not improved significantly from one generation to the next. As this trend continues, Micron two-plane commands offer a ready alternative for improving NAND Flash READ, PROGRAM, and ERASE performance.

Two-plane commands used with interleaved die operations also offer additional READ, PROGRAM, and ERASE performance improvements in Micron NAND Flash devices that support two-plane commands and interleaved die operations. These device features are described in detail in the data sheet for each Micron NAND Flash device with interleaved die operation functionality.

For the latest information on Micron NAND Flash products, refer to the Micron NAND Flash Web site at [www.micron.com/products/nand/](http://www.micron.com/products/nand/).



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**Revision History**

**Rev. B** ..... **9/08**

- Table 2, “PAGE READ 00h-30h vs. TWO-PLANE PAGE READ 00h-00h-30h,” on page 4: In the “Time per Cycle” column for the rows “Read data cycles (page size),” “Read data cycles (page size, 1st plane),” and “Read data cycles (page size, 2nd plane),” changed the value from 25 $\mu$ s to 25ns.
- Table 3, “PROGRAM PAGE 80h-10h vs. TWO-PLANE PROGRAM PAGE 80h-11h-80h-10h,” on page 5: In the “Time per Cycle” column for the rows “Read data cycles (page size),” “Read data cycles (page size, 1st plane),” and “Read data cycles (page size, 2nd plane),” changed the value from 25 $\mu$ s to 25ns.
- Table 4, “PROGRAM PAGE CACHE MODE 80h-15h vs. TWO-PLANE PROGRAM PAGE CACHE MODE 80h-11h-80h-15h,” on page 6: In the “Time per Cycle” column for the rows “Read data cycles (page size),” “Read data cycles (page size, 1st plane),” and “Read data cycles (page size, 2nd plane),” changed the value from 25 $\mu$ s to 25ns.

**Rev. A** ..... **6/07**

- Initial release.