

NAND Flash Status Register Response in Cache Programming Operations

Introduction

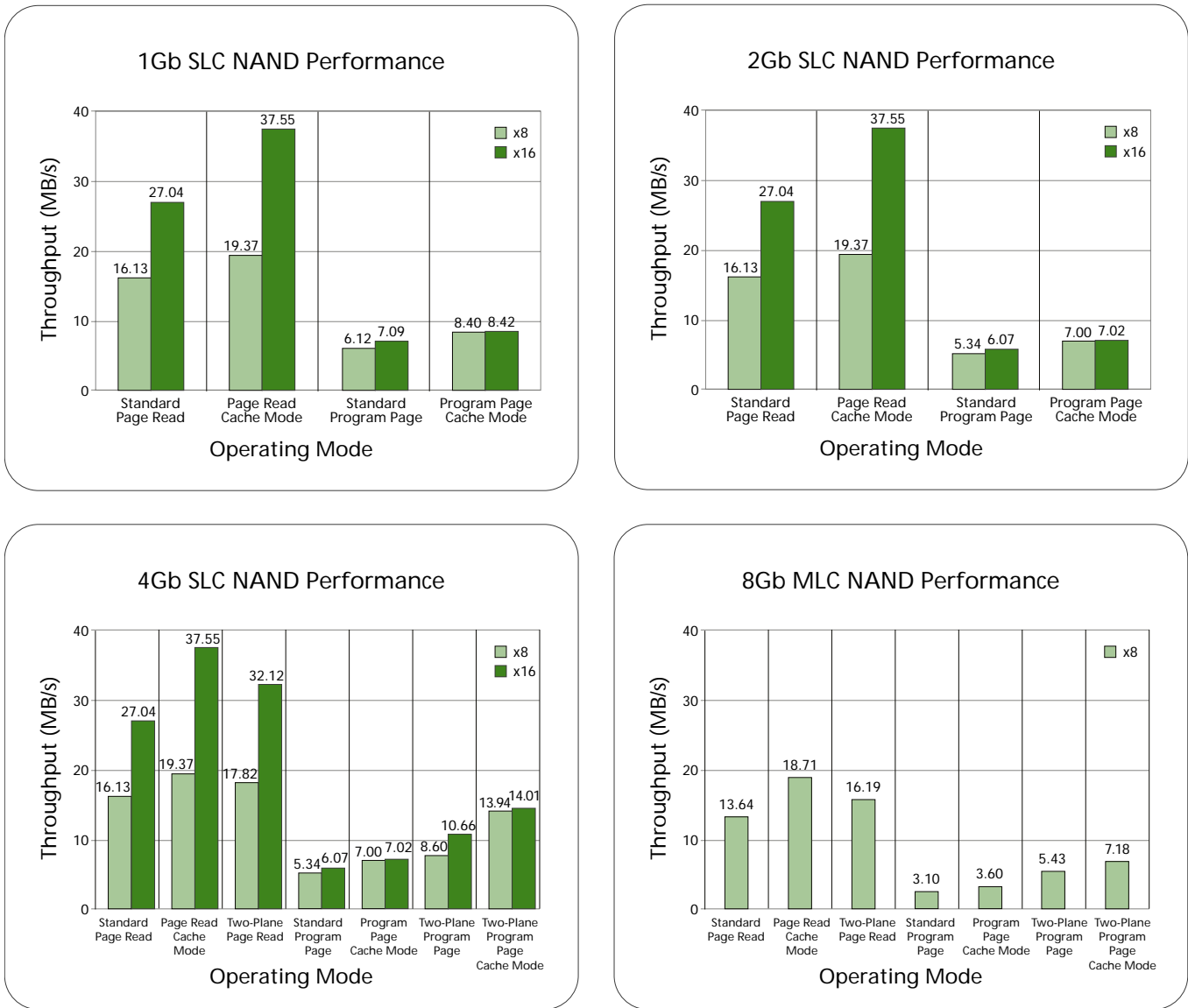
As NAND Flash memory continues to expand into different applications, faster data throughput is required. To enhance data throughput performance, Micron incorporates a cache-read mode and cache-program mode into NAND Flash memory devices.

Systems using cache modes can achieve up to 10 MB/s of read throughput improvement and up to 5 MB/s of program throughput improvement compared to standard page read and program operations (see Figure 1 on page 2). Designers should note, however, that in cache programming mode, status register responses differ from standard page programming responses.

This technical note describes status register responses when operating in cache programming modes.

For additional information on Micron® cache modes, please refer to Micron Technical Notes TN-29-01 (NAND Flash Performance Increase Using the Micron PAGE READ CACHE MODE Command) and TN-29-14 (NAND Flash Performance Increase with PROGRAM PAGE CACHE MODE Command) on Micron's Web site.

Figure 1: NAND Flash Cache Performance Comparison



Cache Mode Architecture

When operating in cache mode, Micron NAND Flash devices use two registers, a data register and a cache register (see Figure 2). During standard page operations, the data and cache registers operate together as a single register. During cache operations, the data and cache registers operate independently, in a pipelined fashion, to increase data throughput.

Cache Program Operations

During a cache programming operation, data is serially clocked into the cache register by toggling WE#; this operation is primarily controlled by timing parameter t_{WC} . After the cache register is loaded—indicated by the CACHE PROGRAM CONFIRM (15h) command and the rising edge of WE#—data is transferred from the cache register to the data register, freeing the cache register for the next programming operation. This operation is primarily controlled by timing parameter t_{CBSY} .

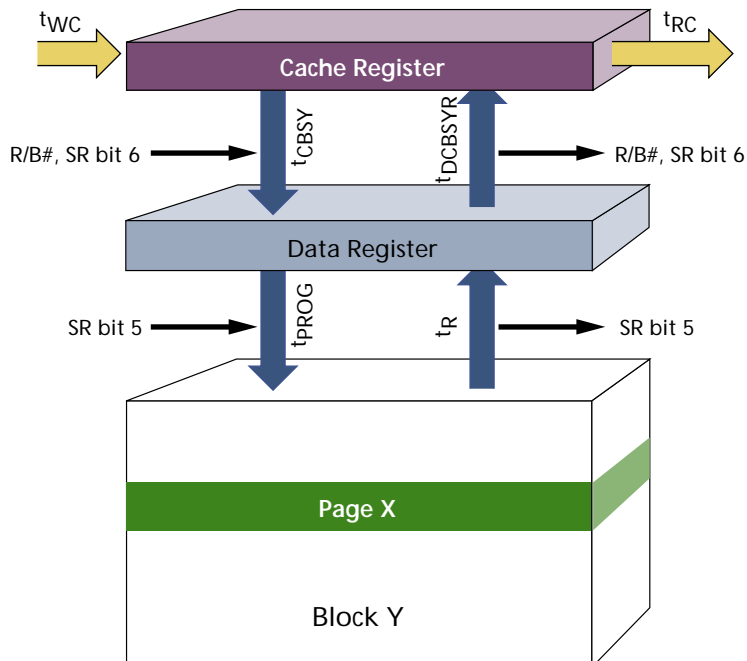
After the data is transferred into the data register, the contents of the data register are programmed to the NAND Flash array, specifically to the addressed page. This operation is primarily controlled by timing parameter t_{PROG} (see Figure 2).

Cache Read Operations

During a cache read operation, data is transferred from the addressed page of the NAND Flash array into the data register. This operation is primarily controlled by timing parameter t_R . After the page is transferred into the data register, the data is transferred from the data register to the cache register. This operation is primarily controlled by timing parameter t_{DCBSYR} .

After the data is loaded into the cache register, it is serially clocked out by toggling RE#. This operation is primarily controlled by timing parameter t_{RC} (see Figure 2).

Figure 2: Cache Operation



Cache Examples

This section provides example cache programming operations. These examples represent only one method for executing a cache operation, and are provided for illustration purposes only. They are intended to convey a possible scenario when reading or monitoring the status register during a cache programming operation.

For cache operations, status register bits 2, 3, and 4 can be ignored; these bits are tied LOW (“0”). In this example, bit 7 is assumed to be HIGH (“1”), with no write protect. Bit 6 indicates the status of the cache register and tracks ready/busy (R/B#). Bit 5 indicates the status of the data register. See Figure 2 on page 3 for details. Bit 1 indicates the status of the previous programming operation. Bit 0 indicates the status of the current operation (see Table 1 and Figure 3).

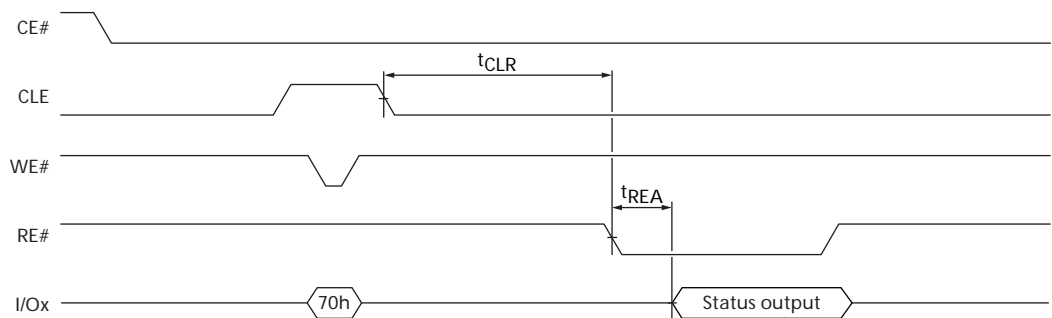
The “current operation” is defined as the program operation that corresponds to the page addressed most recently by the host. The “previous operation” is based on the address issued just prior to the defined current operation.

Table 1: Status Register Bit Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0	Pass/fail	Pass/fail (N)	–	–	Pass/fail	0 = Successful PROGRAM/ERASE 1 = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	0 = Successful PROGRAM 1 = Error in PROGRAM
2	–	–	–	–	–	0
3	–	–	–	–	–	0
4	–	–	–	–	–	0
5	Ready/busy	Ready/busy ¹	Ready/busy	Ready/busy ¹	Ready/busy	0 = Busy 1 = Ready
6	Ready/busy	Ready/busy cache ²	Ready/busy	Ready/busy cache ²	Ready/busy	0 = Busy 1 = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected

- Notes: 1. Status register bit 5 is “0” during the actual programming operation. If cache mode is used, this bit will be “1” when all internal operations are complete.
2. Status register bit 6 is “1” when the cache is ready to accept new data. R/B# follows bit 6.

Figure 3: Status Register Operation



Cache Programming Example

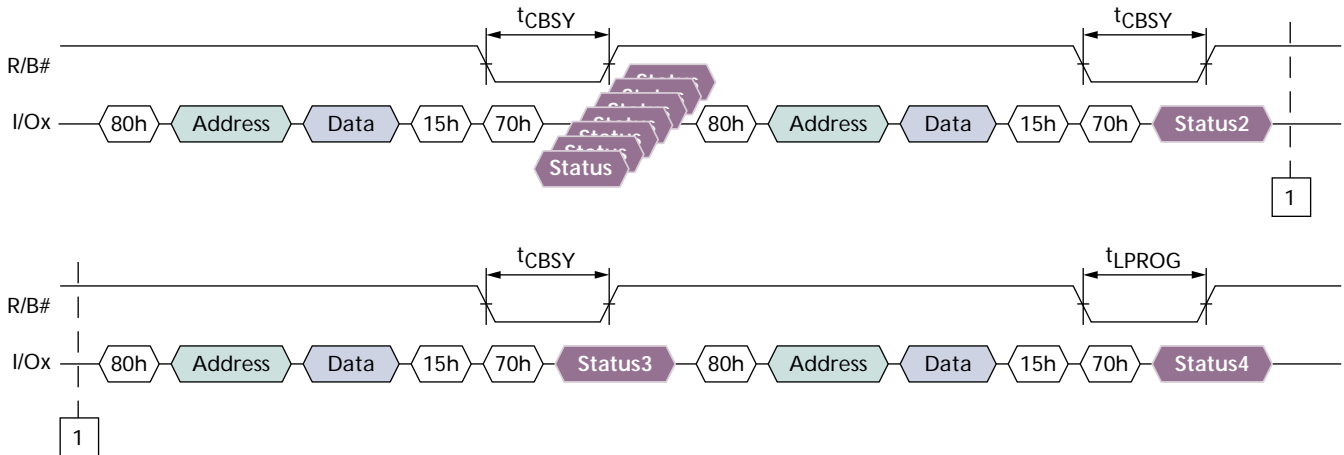
An example of a possible cache programming operation is shown in Figure 8 on page 9. In this example, the required 80h-address-data-15h sequence is executed. This sequence represents the successful execution of the PROGRAM PAGE CACHE MODE command described in Micron NAND Flash data sheets.

PROGRAM PAGE CACHE MODE Operation and Responses

Upon successful completion of the PROGRAM PAGE CACHE MODE command, R/B# goes LOW to indicate that the device is busy transferring data from the cache register to the data register. For the duration of this busy time (t_{CBSY}), the system can poll the NAND Flash status register using the 70h-Status1 command sequence shown in Figure 8. See Micron Technical Note TN-29-13 (Monitoring Ready/Busy Status in 2Gb, 4Gb, and 8Gb Micron NAND Flash Devices) for NAND Flash status register polling guidelines.

Reading the status register is much faster than transferring or programming data, so the system can actually poll or monitor the status register during t_{CBSY} .

Figure 4: Cache Programming Operation and Responses



Cycle 1 Programming (Status1)

During the status register polling or monitoring process, status register responses resemble those provided in Figure 5 and Table 2. As indicated in Table 2, Status1₀ is the initial status response immediately following the PROGRAM PAGE CACHE MODE command; Status1₄ is the fifth response and indicates that the cache register is ready.

As would be expected, the device is initially busy moving data from the cache register to the data register (Status1₀); this is indicated by the 8xh status register response. While the data transfer is occurring, bits 5 and 6 of the status register indicate the status of the data transfer and program operations. Bit 6 tracks R/B# and indicates the status of the cache register. Bit 5 indicates the status of the program operation (see Figure 2 on page 3).

Successive polling or monitoring of the status register generates responses similar to the initial check (see Table 2). At some point, bit 6 of the status register (and R/B#) goes from a busy state (“0”) to a ready state (“1”). Status1₄ indicates that the cache register is ready to accept another transfer operation. Loading the cache register while the data register is busy programming provides increased throughput using the cache programming mode.

In cache programming mode, the system is capable of polling or monitoring until status register bit 1 is ready (Status1_n). However, this approach effectively eliminates the performance advantages of the cache programming mode because it inhibits cache loading while the data register is busy. It is best to wait until bit 1 is ready (“1”).

Figure 5: Cache Program Status1 Example

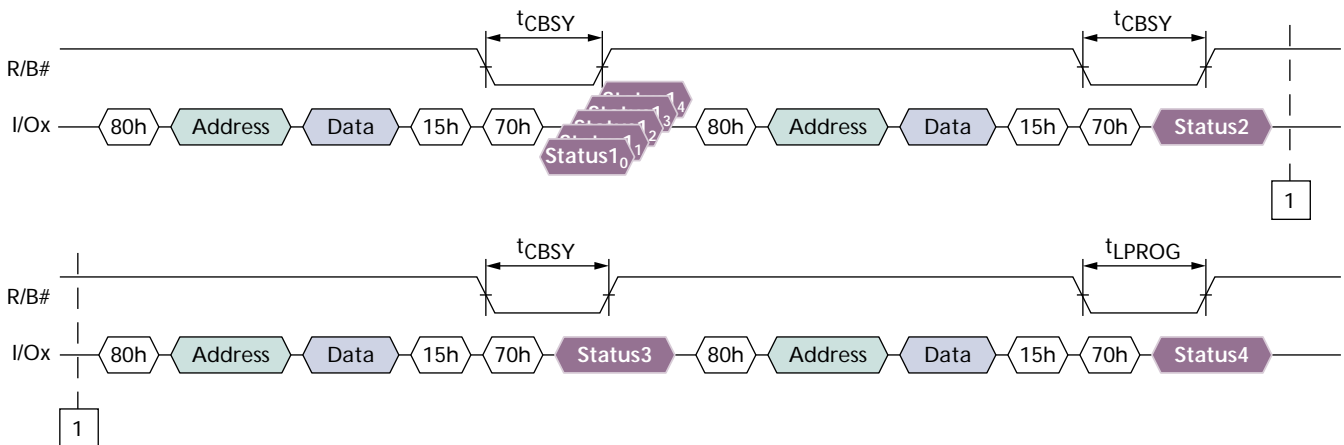


Table 2: Cache Program Status Bit 1 Responses

Status1 Bit	7	6	5	4	3	2	1	0	Value	Comments
Status1 ₀	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status1 ₁	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status1 ₂	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status1 ₃	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status1 ₄	1	1	0	0	0	0	0	x	C0 or C1	Cache ready, program busy, assume previous operation was successful (i.e., no errors exist)
...	1	1	0	0	0	0	0	x	C0 or C1	Cache ready, program busy, assume previous operation was successful (i.e., no errors exist, reflected by bit 1)
Status1 _n	1	1	1	0	0	0	0	0	E0h	Cache ready, program ready, no errors

Cycle 2 Programming (Status2)

When the cache register response indicates a ready status via Status1₄, the second PROGRAM PAGE CACHE MODE command is executed. Status register polling or monitoring occurs in Status2, the same as in Status1 (see Figure 6 and Table 3), with similar responses in Status2 (see Figure 6 and Table 3).

Error Tracking

To better understand how an error is tracked while performing a cache program operation, assume that a programming error has occurred in the second programming cycle.

When bit 6 is LOW or busy, bit 1 is undefined; when bit 6 is HIGH or ready, bit 1 is valid.
 When bit 5 is LOW or busy, bit 0 is undefined; when bit 5 is HIGH or ready, bit 0 is valid.

Figure 6: Cache Program Status2 Example

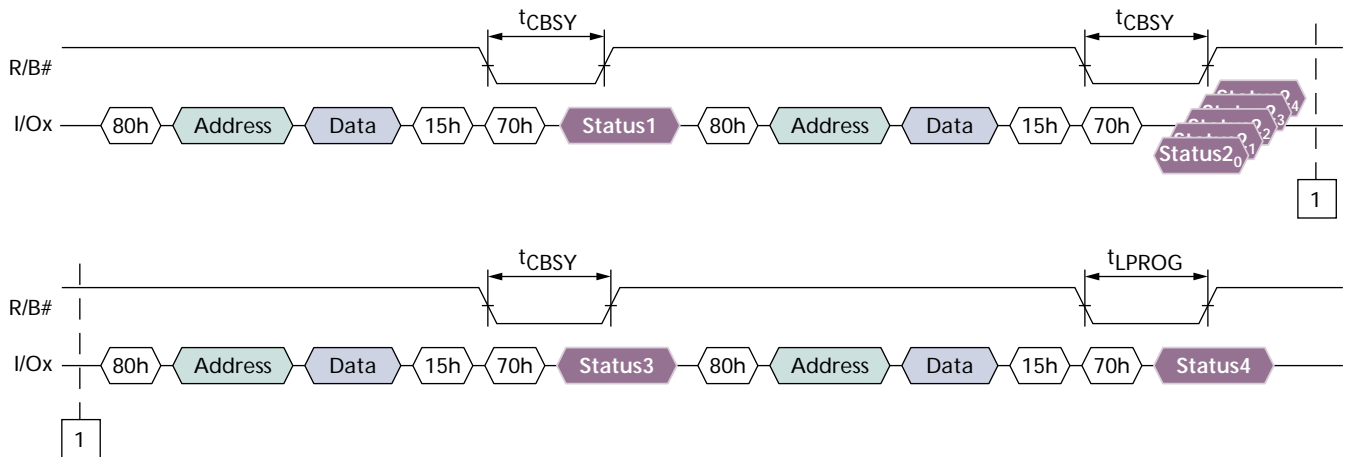


Table 3: Cache Program Status2 Bit Responses

Status2 Bit	7	6	5	4	3	2	1	0	Value	Comments
Status2 ₀	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status2 ₁	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status2 ₂	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status2 ₃	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status2 ₄	1	1	1	0	0	0	0	x	C0h or C1h	Cache ready, program busy, first cache program had no error

Cycle 3 Programming (Status3)

Similar to the first cache programming cycle, when Status2 indicates that the cache register is ready, a third PROGRAM PAGE CACHE MODE command is executed. Register polling or monitoring also occurs in Status3. In Status3, when status register bit 6 indicates that the cache register is ready for another load, status register bit 1 reflects the programming error encountered during the second programming cycle (see Figure 7, Table 4, and Figure 8 on page 9).

When an error occurs in a system environment, an error-handling routine should be invoked to address the error. In cache programming mode, error reporting lags one operation cycle or step behind where the error actually occurred. This delay must be taken into account when implementing error management.

When Status3 indicates that the cache register is ready, a fourth PROGRAM PAGE CACHE MODE command is executed. The status register polls or monitors the operation. When status register bit 6 indicates that the cache register is ready for another load, status register bit 1 reflects the programming status of the third programming step.

Figure 7: Cache Program Status3

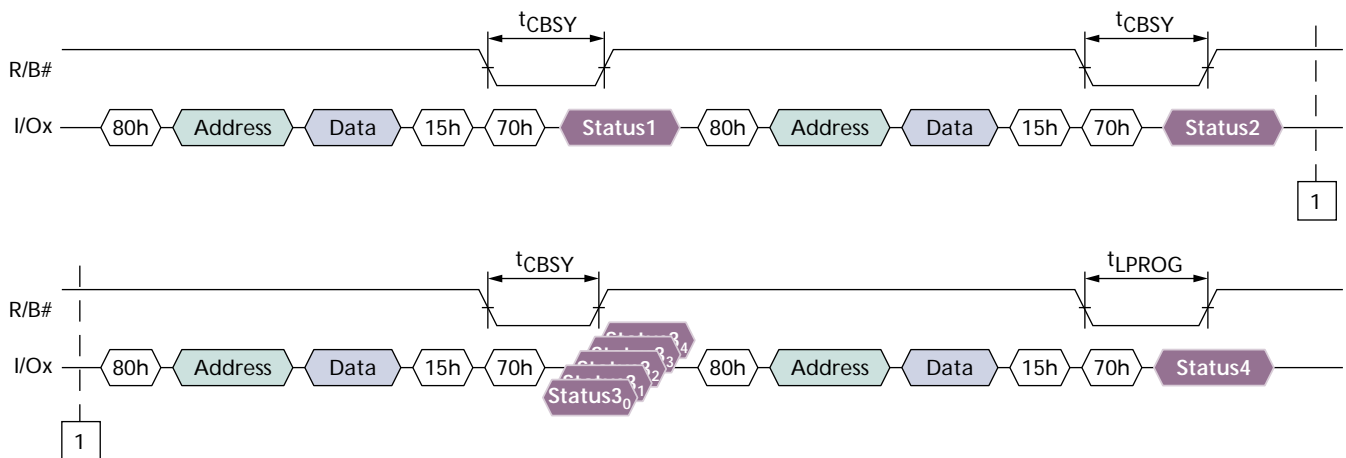


Table 4: Cache Program Status3 Bit Responses

Status3 Bit	7	6	5	4	3	2	1	0	Value	Comments
Status3 ₀	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status3 ₁	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status3 ₂	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status3 ₃	1	0	0	0	0	0	x	x	8xh	Cache busy, program busy
Status3 ₄	1	1	0	0	0	0	1	x	C2h or C3h	Cache ready, program busy, second cache program had an error

Cycle 4 Programming (Status4)

Status4 is the last cache programming operation, so the status register should be polled until bits 5 and 6 are ready, which indicates that the fourth and final cache program operation has completed (see Figure 8 and Table 5).

Figure 8: Cache Program Status4

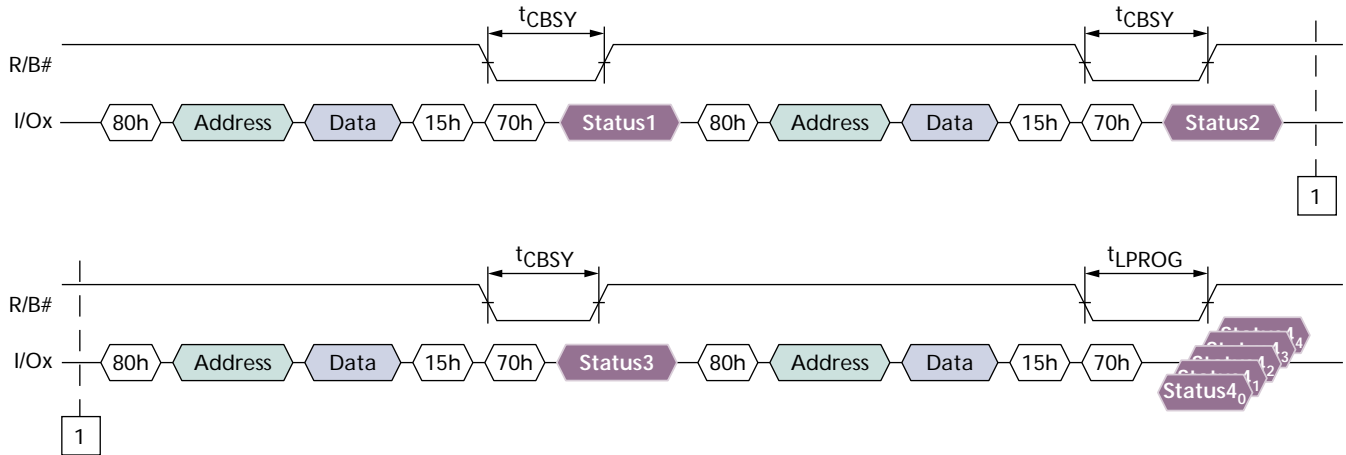


Table 5: Cache Program Status4 Bit Responses

Status4 Bit	7	6	5	4	3	2	1	0	Value	Comments
Status4 ₀	1	0	0	0	0	0	x	x	82h or 83h	Cache busy, program busy, no errors
Status4 ₁	1	0	0	0	0	0	x	x	82h or 83h	Cache busy, program busy, no errors
Status4 ₂	1	0	0	0	0	0	x	x	82h or 83h	Cache busy, program busy, no errors
Status4 ₃	1	0	0	0	0	0	x	x	82h or 83h	Cache busy, program busy, no errors
Status4 ₄	1	1	0	0	0	0	0	x	C0h or C1h	Cache ready, program busy, no errors
Status4 ₅	1	1	1	0	0	0	0	0	E0h	Cache ready, program ready, no errors

Summary

In cache programming mode, status register responses differ from standard page programming responses. With proper status register execution that recognizes these differences, system designers can achieve significantly improved throughput performance using Micron NAND Flash cache programming operations versus standard page programming operation performance.



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